1.3 Power MOSFET

The metal oxide semiconductor field effect transistors (MOSFET) are majority carrier devices. Fig. 1.3.1 shows the symbols of MOSFETs.

Observe that there are two types of power MOSFETs : n-channel MOSFET and p-channel MOSFET. The MOSFET has three terminals : gate (G), drain (D) and source (S).

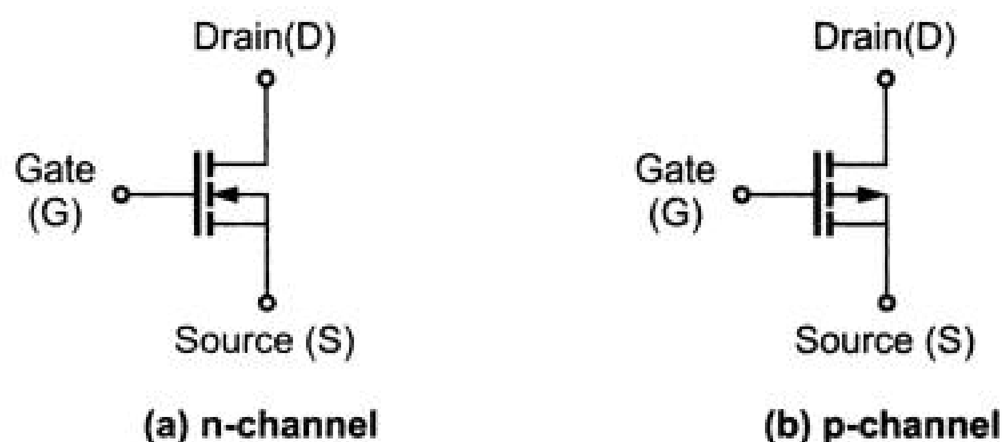


Fig. 1.3.1 Symbols of MOSFETs

When the MOSFET is turned 'on' the current flows from drain to source. The voltage is applied between gate-source to turn 'on' the MOSFET. Very small current flows from gate to source. Only voltage is to be applied to turn-on the MOSFET. The MOSFET can be turned-off by removing the gate to source voltage. Thus gate has full control over the conduction of the MOSFET. The turn-on and turn-off times of MOSFETs are very small. Hence they operate at very high frequencies. Hence MOSFETs are preferred in applications such as choppers and inverters. Since only voltage drive (gate-source) is required, the drive circuits of MOSFETs are very simple. The paralleling of MOSFETs is easier due to their positive temperature coefficient (PTC). MOSFETs have high on-state resistance, $R_{DS(on)}$. Hence for higher currents, losses in the MOSFETs are substantially increased. Hence MOSFETs are mainly used for low power applications.

1.3.1 Construction and Operation of Power MOSFETs

[May-2004, Nov.-2007, May-2008, Dec.-2008]

1.3.1.1 Basic Structures of Power MOSFET

There are two types of MOSFETs : depletion type MOSFET and enhancement type MOSFET. In both of these types the MOSFETs can be n-channel or p-channel. Fig. 1.3.2 shows the structure of n-channel enhancement type MOSFET. The source and drain are connected to n^+ regions. These regions are heavily doped with the intensity of 10^{19} per cm^3. The p-type body region forms the channel between drain and source. The body region has the doping level of 10^{16} per cm^3. The gate is not directly connected to the p-type

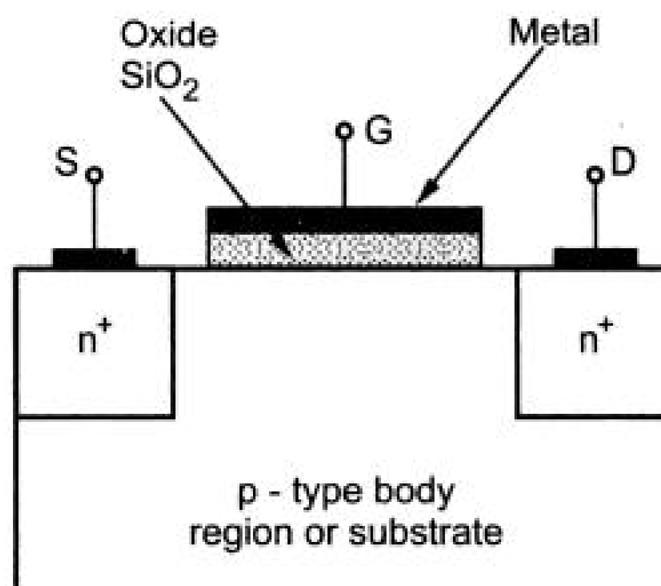


Fig.1.3.2 Structure of n-channel enchancemode MOSFET (Drift layer is not shown.)

Copyrighted material

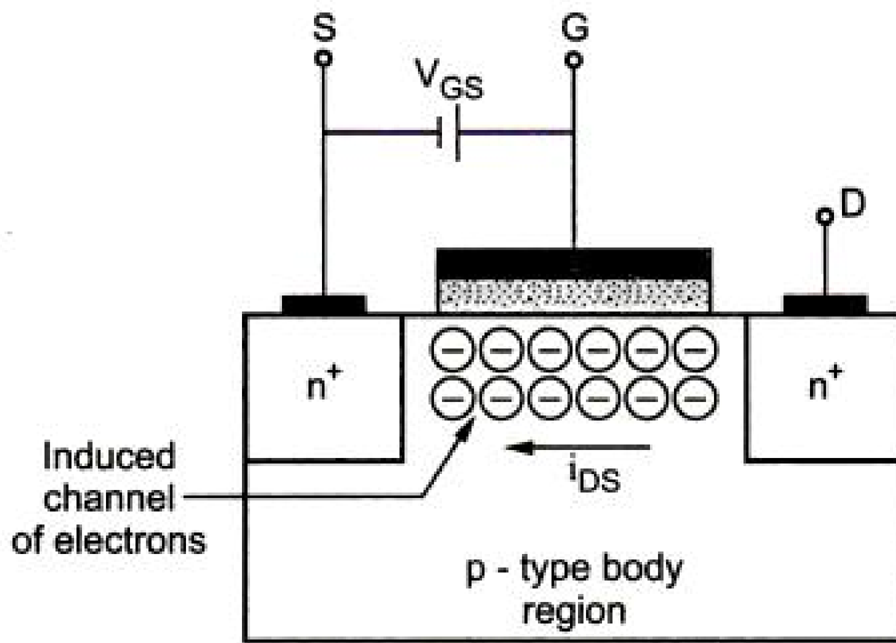


Fig. 1.3.3 Formation of inversion layer or channel

region. There is insulating oxide (SiO_2) layer between gate metal and p-type layer. When gate is made positive with respect to source, an accumulation layer is formed in the channel as shown in Fig. 1.3.3. This accumulation layer is formed because of V_{GS}. The gate terminal (metal) is positive. The other side of oxide layer is p-type of body region. Accumulation layer of electrons is generated in the body region near oxide layer. This is also called induced channel of electrons. Therefore current (i_{DS}) starts flowing through this induced channel. The current flows from drain to source. If V_{GS} = 0, then induced channel is absent and no current flows. Since channel is made of electrons, this is called n-channel MOSFET.

1.3.1.2 Vertical Structure of Four Layer Power MOSFET

Answer following question after reading this topic.

1. *Draw vertical structure of power MOSFET and explain its operation.*

Marks [4], May-2004; Marks [8], Dec.-2007; Marks [3], May-2008; Marks [5], Dec.-2008

Most likely and **asked in** previous University Exam

Fig. 1.3.4 shows the vertically diffused power MOSFET that has four layers. It is $n^+ pn^- n^+$ structure. It is n-channel enhancement mode MOSFET. The n^+ regions are heavily doped (10^{19} per cm^3). The p-type middle layer is called body region. It has the doping level of 10^{16} per cm^3. The channel for conduction is established in this region. The n^- region is called drift region. It is lightly doped (10^{14} per cm^3). The breakdown voltage of the device depends upon this drift region. (Refer Fig. 1.3.4 on next page.)

Advantages of vertical structure

1. On-state resistance of MOSFET is reduced.
2. Width of the gate is maximized. Hence, gain of the device is increased.

Copyrighted material

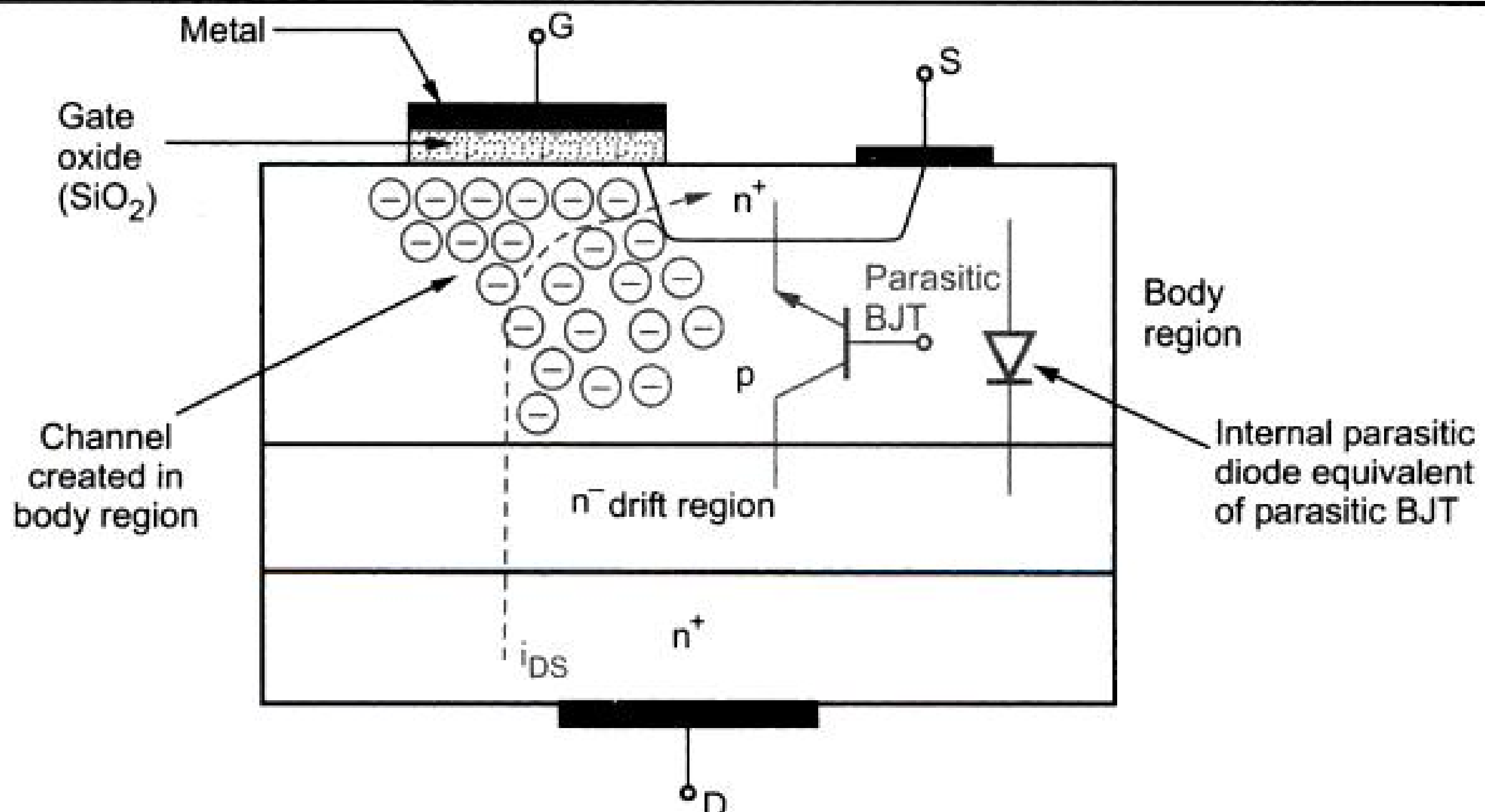


Fig. 1.3.4 Four layer structure of n-channel enhancement mode MOSFET

1.3.1.3 Operation of Power MOSFET

In the Fig. 1.3.4 structure observe that the source is connected to n^+ region as well as p-type body region. The gate also overlaps p-type region and n^+ region. The gate is isolated from these regions by SiO_2 layer. When V_{GS} is positive, an n-type channel is induced in the body region as shown in Fig. 1.3.4. Hence current (i_{DS}) starts flowing from drain to source as shown. Because of drift region, the on-state drop of MOSFET increases.

1.3.1.4 Body to Source Short

Answer following question after reading this topic.

1. *Explain the reason for "body-source-short" in MOSFET structure.* **Marks [2], May-2004; May-2008, Dec.-2008**

Most likely and **asked in** previous University Exam

In Fig. 1.3.4 observe that a parasitic BJT is formed as shown. Base of this parasitic BJT is the p -type body region. Emitter is n^+ region and collector is n^- drift region. The emitter and base of this parasitic BJT are shorted to source. Hence it does not conduct. This is the reason for shorting p-type body region to source.

1.3.1.5 Integral Reverse Diode

Answer following questions after reading this topic.

1. *External antiparallel diodes are not connected across the power MOSFETs used in an inverter- Give reason.* **Marks [2], Dec.-2007**
2. *Explain the presence of integral reverse diode in the structure of power MOSFET .* **Marks [2] May-2004, May-2008, Dec.-2008**

Most likely and **asked in** previous University Exam

Copyrighted material

The parasitic BJT actually performs the function of diode. This parasitic diode is shown symbolically in Fig. 1.3.4. This parasitic diode is formed between drain and source of the MOSFET.

Use of internal parasitic diode

The parasitic diode conducts in reverse direction compared to direction of conduction of MOSFET. In inverters with inductive load, the reverse current flows through this parasitic diode. There is no need to connect external reverse diode.

1.3.2 Steady State (V-I) Characteristics of MOSFETs

Answer following question after reading this topic.

1. *Explain the steady state characteristics of MOSFET.*

Most likely and **Important** Question

Fig. 1.3.5 shows the V-I characteristics of n-channel power MOSFET. The drain current i_D is plotted with respect to drain to source voltage v_{DS}. These characteristics are plotted for various values of gate source voltages (V_{GS}). In Fig. 1.3.5 observe that there are three

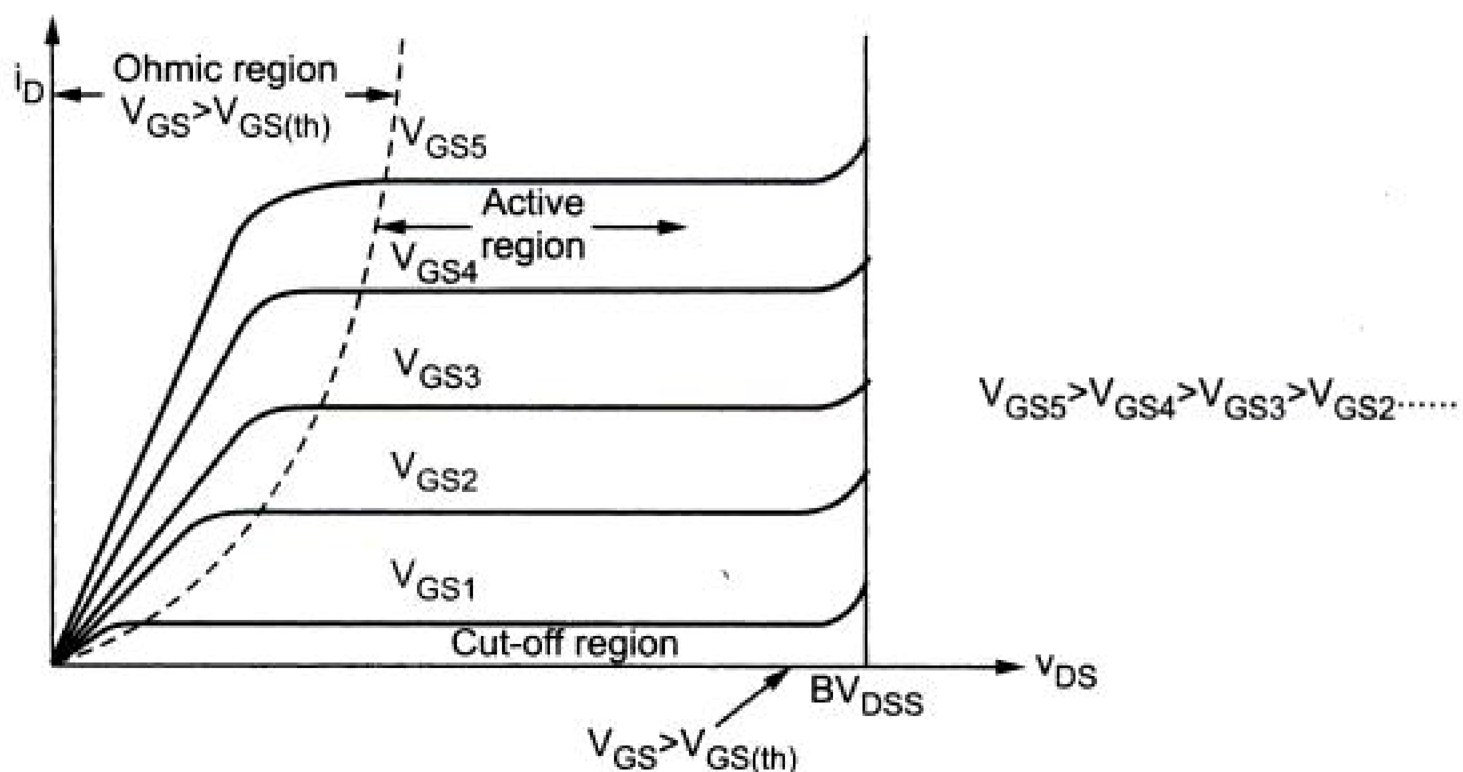


Fig. 1.3.5 V-I characteristics of n-channel power MOSFET

regions in the characteristics : Ohmic region, active region and cut-off region. In the cut-off region, the drain current is negligible and the MOSFET is said to be in 'OFF' state. The MOSFET is driven in cut-off region by applying $V_{GS} < V_{GS(th)}$. Here $V_{GS(th)}$ is the threshold gate source voltage. When gate to source voltage is less than threshold gate source voltage, MOSFET is off, i.e. in cut-off region. The MOSFET is driven into ohmic

Copyrighted material

region when $V_{GS} >> V_{GS(th)}$. In the ohmic region, the MOSFET conducts heavily. Hence it is said to be 'on' in the ohmic region. Thus by applying heavy gate to source voltage, MOSFET can be turned on. In the power electronic applications, MOSFET is never operated in the active region. In active region it acts as an amplifier. For switching applications, MOSFET is operated only in ohmic and cut-off regions. The BV_{DSS} is the drain to source breakdown voltage, when the gate is open circuited. The MOSFET is damaged if drain to source voltage is increased above BV_{DSS}.

1.3.3 Switching Characteristics of MOSFET

Answer following question after reading this topic.

1. *Explain the switching characteristics of MOSFET.*

Most likely and **Important** Question

The internal capacitances of MOSFET affect the turn-on and turn-off times of MOSFETs. These capacitances have no effect during steady state. Fig. 1.3.6 shows the switching model of MOSFET.

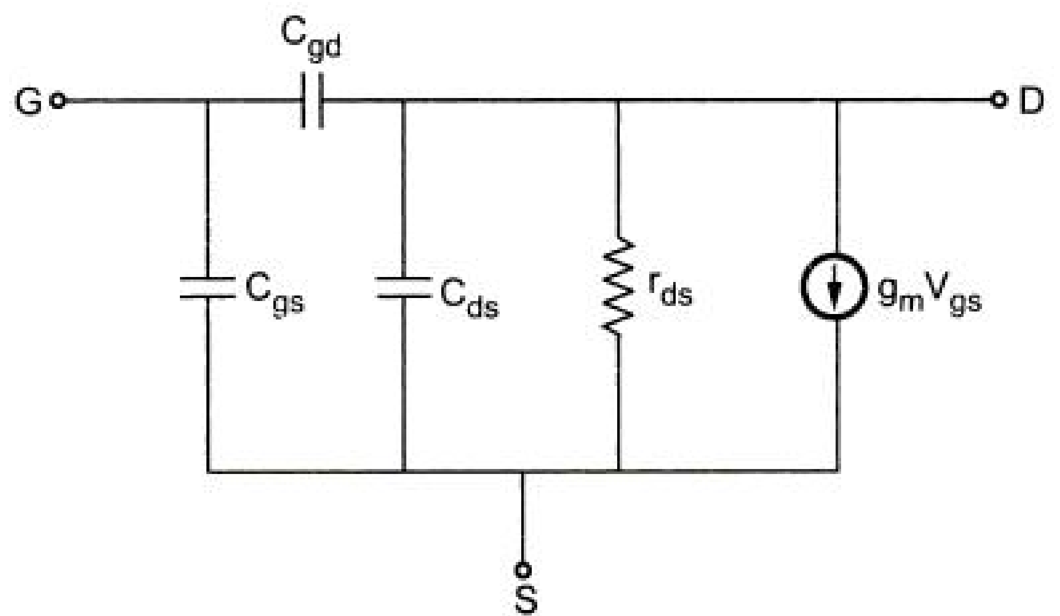


Fig. 1.3.6 Switching model of MOSFET

In the Fig. 1.3.6 C_{gs} is the gate to source parasitic capacitance and C_{gd} is the gate to drain parasitic capacitance. The MOSFET can be turned on by applying positive gate voltage as shown in Fig. 1.3.7.

When the gate voltage is applied, the gate to source capacitance C_{gs} starts charging. The *turn-on delay* ($t_{d(on)}$) is the time required to charge C_{gs} to threshold voltage (V_T). After this voltage, the drain current (i_D) starts rising. The C_{gs} charges from threshold voltage to full gate voltage (V_{gsp}). The time required for this charging is called *rise time* (t_r). Observe that during this period, the drain current rises to its full value, i.e. I_o. The MOSFET is then said to have fully turned on. Thus, the total turn-on time of the MOSFET is,

$$t_{on} = t_{d(on)} + t_r$$

Copyrighted material

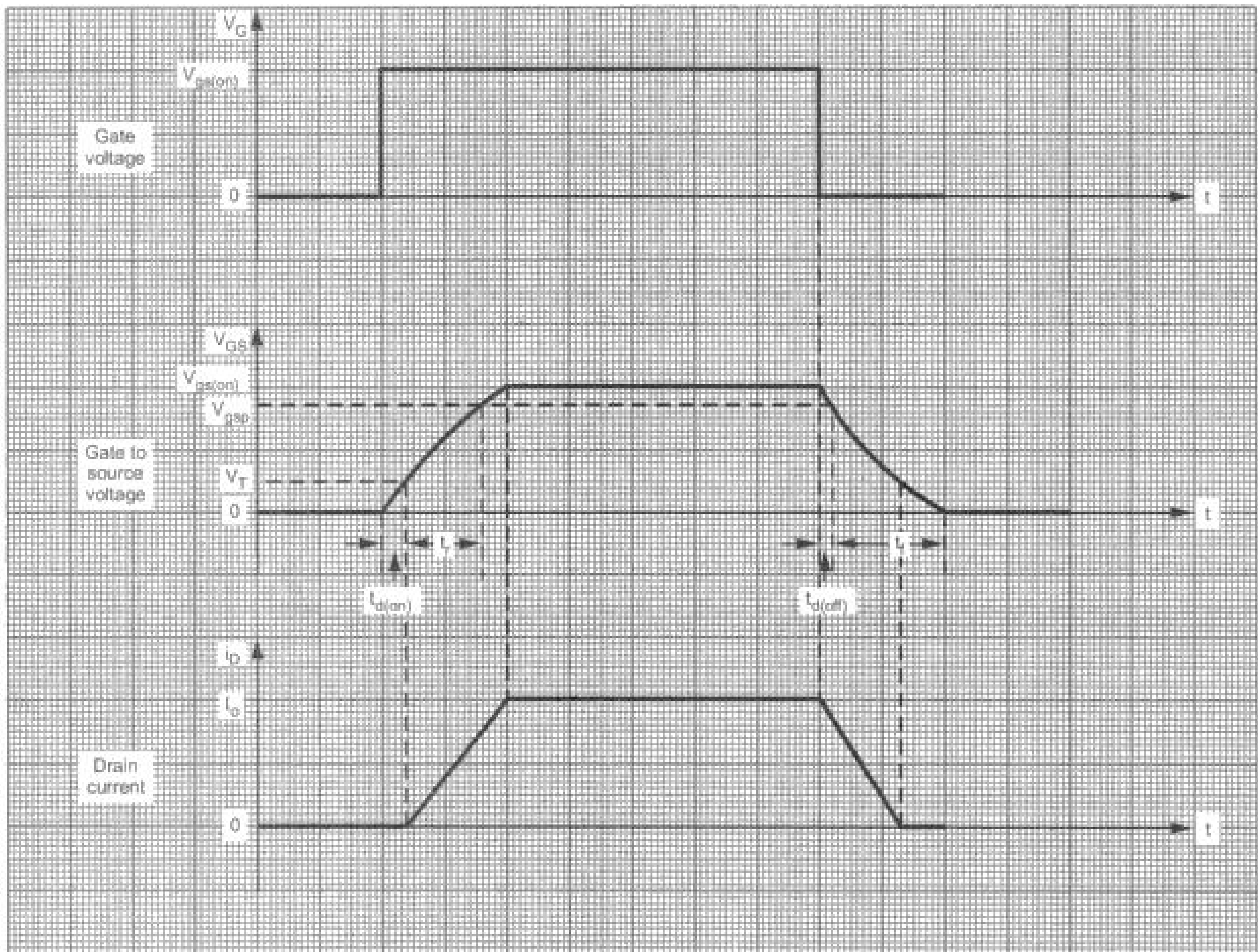


Fig. 1.3.7 Switching characteristics of MOSFET

To turn-off the MOSFET, the gate voltage is made negative or zero. The gate to source voltage then reduces from $V_{gs(on)}$ to V_{gsp}. That is, C_{gs} discharges from overdrive to pinch-off region gate voltage. The time required for this discharge is called *turn-off delay* time ($t_{d(ff)}$). The drain current also start reducing. The C_{gs} keeps on discharging and its voltage becomes equal to threshold voltage (V_T). The time required to discharge C_{gs} from V_{gsp} to V_T is called *fall time* (t_f). The drain current becomes zero when $v_{GS} \leq V_T$. The MOSFET is then said to have turned-off. The C_{gs} then discharges to zero voltage. The turn-off time of the MOSFET is equal to sum of turn-off delay time and fall time. i.e.,

$$t_{off} = t_{d(off)} + t_f$$

1.3.4 Paralleling of MOSFETs

Answer following question after reading this topic.

1. *Justify-Parallel operation of MOSFETs can be done more easily as compared to thyristors.* **Marks[2], Dec.-2002; Marks [4], Dec.-2007**

Most likely and **asked in** previous University Exam

Copyrighted material

MOSFETs have positive temperature coefficient (PTC). If the current increases in a particular MOSFET, due to losses its temperature will rise. This rise in temperature will increase internal resistance of the MOSFET. Due to increased internal resistance, the current through the MOSFET will reduce. If many MOSFETs are connected in parallel, above mechanism tries to balance the currents through the MOSFETs. Thus paralleling of MOSFETs is simple due to their positive temperature coefficient.

In case of other devices such as thyristors, paralleling is not so simple, since thyristors have negative temperature coefficient. This does not help the internal adjustment of equal current through SCRs. In fact external equalizing components are required for paralleling of SCRs.

1.3.5 Merits, Demerits and Applications of MOSFETs

1.3.5.1 Merits of MOSFETs

Answer following questions after reading this topic.

1. *Why MOSFET is used in high frequency applications ?*
   Marks [4], Dec.-2007
2. *Power MOSFET is best switch in PWM inverter. Justify.*
   Marks [2], Dec.-2006

Most likely and **asked in** previous University Exam

i. MOSFETs are majority carrier devices.

ii. MOSFETs have positive temperature coefficient, hence their paralleling is easy.

iii. MOSFETs have very simple drive circuits, since they have insulated gate. Such circuits can be easily designed for high frequency operation.

iv. MOSFETs have short turn-on and turn-off times, hence they operate at high frequencies.

v. MOSFETs do not require commutation circuits.

vi. Gate has full control over the operation of MOSFET.

vii. PWM inverters require high switching frequencies. Since MOSFETs operate at high frequencies, they are best suitable for PWM inverters.

1.3.5.2 Demerits of MOSFETs

i. On-state losses in MOSFETs are high.

ii. MOSFETs are used only for low power applications.

iii. MOSFETs suffer from static charge.

Copyrighted material

1.3.5.3 Applications of MOSFETs

i. High frequency and low power inverters.

ii. High frequency SMPS.

iii. High frequency inverters and choppers.

iv. Low power AC and DC drives.

Sr. No.	BJT	MOSFET
1.	This is bipolar device.	This is majority carrier device.
2.	Controlled by base.	Controlled by gate.
3.	Current controlled device.	Voltage controlled device.
4.	Negative temperature coefficient.	Positive temperature coefficient.
5.	Paralleling of BJTs is difficult.	Paralleling of MOSFETs is simple.
6.	Losses are low.	Losses are higher than BJTs.
7.	Drive circuit is complex.	Drive circuit is simple.
8.	Switching frequency is lower than MOSFET.	Switching frequency is high.
9.	BJTs are suitable for high power applications.	MOSFETs are suitable for low power application.
10.	BJTs are available with higher voltage and current ratings.	MOSFETs have less voltage and current ratings.

Table 1.3.1 Comparison of BJT and MOSFET **[Dec.-2000]**

1.3.6 Safe Operating Area (SOA) of Power MOSFET

Answer following question after reading this topic.

1. *Explain SOA of power MOSFET.* **Marks [2], May-2008**

Most likely and **asked in** previous University Exam

Fig. 1.3.8 shows the safe operating area (SOA) of the power MOSFET.

- The maximum drain current is I_{DM} and breakdown drain to source voltage is BV_{DSS}.

Copyrighted material

- The maximum junction temperature $T_{j\,max}$ sets the thermal limit.
- For power MOSFETs, the forward biased and reverse biased SOA are identical.
- The SOA is almost square of switched mode applications. Hence MOSFETs are preferred at high frequencies.
- The SOA reduces as switching frequency reduces and it is minimum at DC operation.
- There is no second breakdown as compared to power BJT. Hence it does not appear in the SOA.

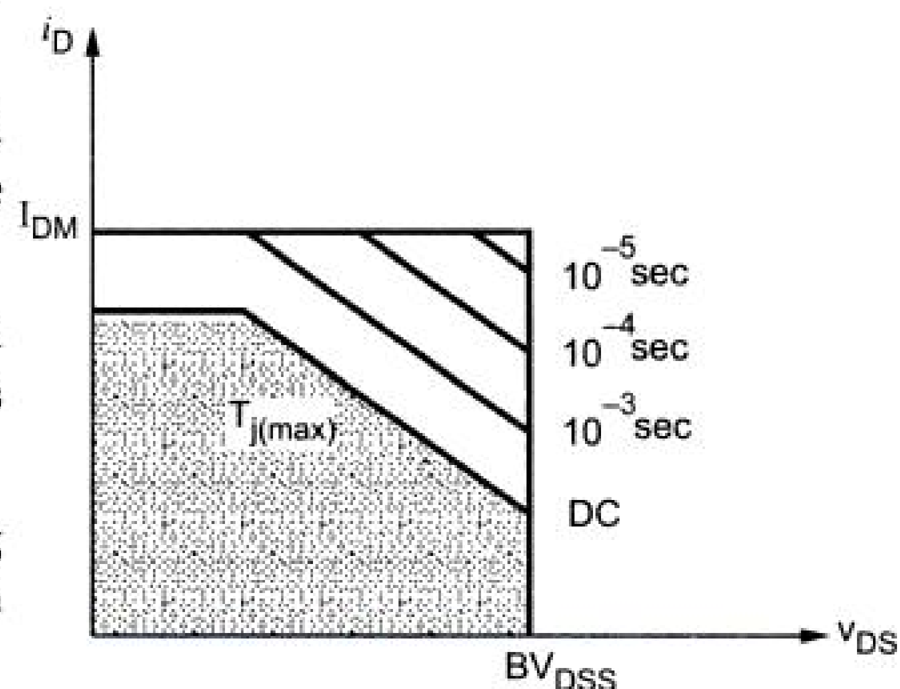


Fig. 1.3.8 SOA of power MOSFET

1.4 IGBT

Answer following question after reading this topic.

1. *Write a short note on IGBT as power device.* **Marks[5], Dec.-2000**

Most likely and **asked in** previous University Exam

The Insulated Gate Bipolar Transistor (IGBT) is the latest device in power electronics. It is obtained by combining the properties of BJT and MOSFET. We know that BJT has lower on-state losses for high values of collector current. But the drive requirement of BJT is little complicated. The drive of MOSFET is very simple (i.e. only voltage is to be applied between gate and source). But MOSFET has high on-state losses. The gate circuit of MOSFET and collector emitter circuits of BJT are combined together to form a new device. This device is called IGBT. Thus IGBT has advantages of both the BJT and MOSFETs. Fig. 1.4.1 shows the symbol of IGBT. Observe that the symbol clearly indicates combination of MOSFET and BJT.

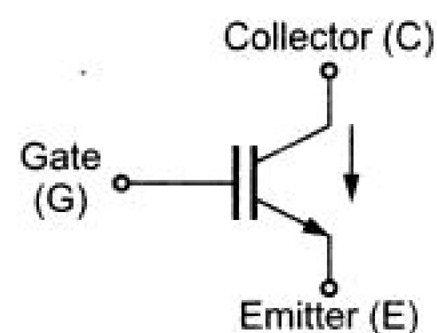


Fig. 1.4.1 Symbol of IGBT

The IGBT has three terminals : Gate (G), collector (C) and emitter (E). Current flows from collector to emitter whenever a voltage between gate and emitter is applied. The IGBT is said to have turned 'on'. When gate emitter voltage is removed, IGBT turns-off. Thus gate has full control over the conduction of IGBT. When the gate to emitter voltage is

Copyrighted material

applied, very small (negligible) current flows. This is similar to the gate circuit of MOSFET. The on-state collector to emitter drop is very small like BJT.

1.4.1 Construction of IGBT

Answer following question after reading this topic.

1. *Draw the vertical cross-section of an IGBT.*
Marks [2], May-2001 ; May-2003 ; Marks [4] Dec.-2004; May-2006; Marks [3] Dec.-2006,

Most likely and **asked in** previous University Exam

The structure of IGBT is similar to that of MOSFET. Fig. 1.4.2 shows the vertical cross-section of IGBT. In this structure observe that there is additional p^+ layer. This layer is collector (Drain) of IGBT.

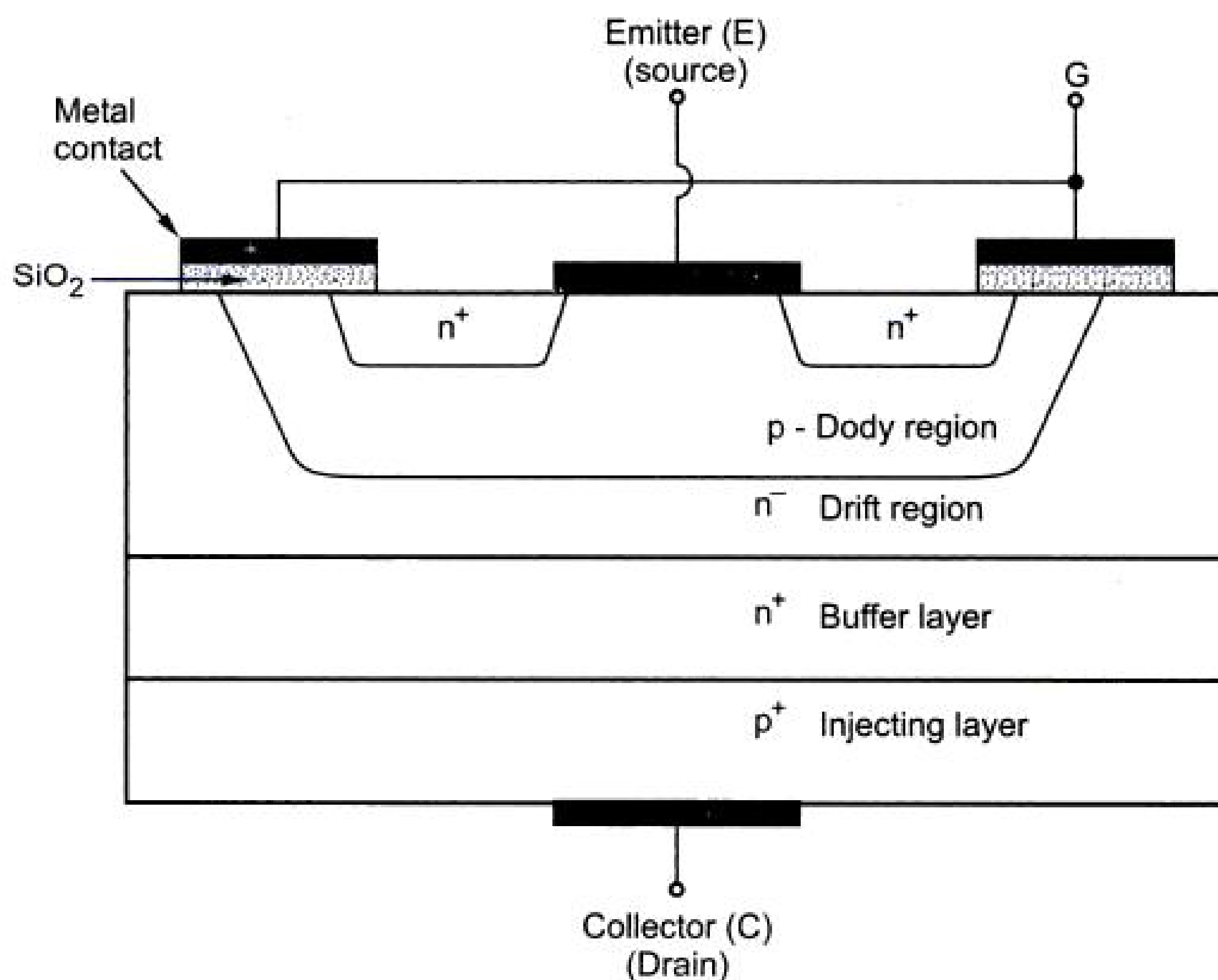


Fig. 1.4.2 Vertical cross-section of IGBT

This p^+ injecting layer is heavily doped. It has the doping intensity of 10^{19}per cm^3. The doping of other layers is similar to that of MOSFET. n^+ layers have 10^{19} per cm^3. p-type body region has doping level of 10^{16} per cm^3. The n^- drift region is lightly doped (10^{14} per cm^3).

Copyrighted material

1.4.1.1 Punch through IGBT

The n^+ buffer layer is not necessary for the operation of IGBT. The IGBTs which have n^+ buffer layer are called punch through IGBTs. Such IGBTs have asymmetric voltage blocking capabilities. Punch through IGBTs have faster turn-off times. Hence they are used for inverter and chopper circuits.

1.4.1.2 Non-punch through IGBT

The IGBTs without n^+ buffer layer are called non-punch through IGBTs. These IGBTs have symmetric voltage blocking capabilities. These IGBTs are used for rectifier type applications.

1.4.1.3 Operation of IGBT

Answer following questions after reading this topic.

1. *The principle of operation of IGBT is similar to that of MOSFET. State true or false and justify.*
2. *Explain the operation of IGBT.*

Most likely and **Important** Questions

Similarity of Operation with MOSFET

Now let us see how IGBT operates. When $V_{GS} > V_{GS(threshold)}$, then the channel of electrons is formed beneath the gate as shown in Fig. 1.4.3. These electrons attract holes from p^+ layer. Hence, holes are injected from p^+ layer into n^- drift region. Thus

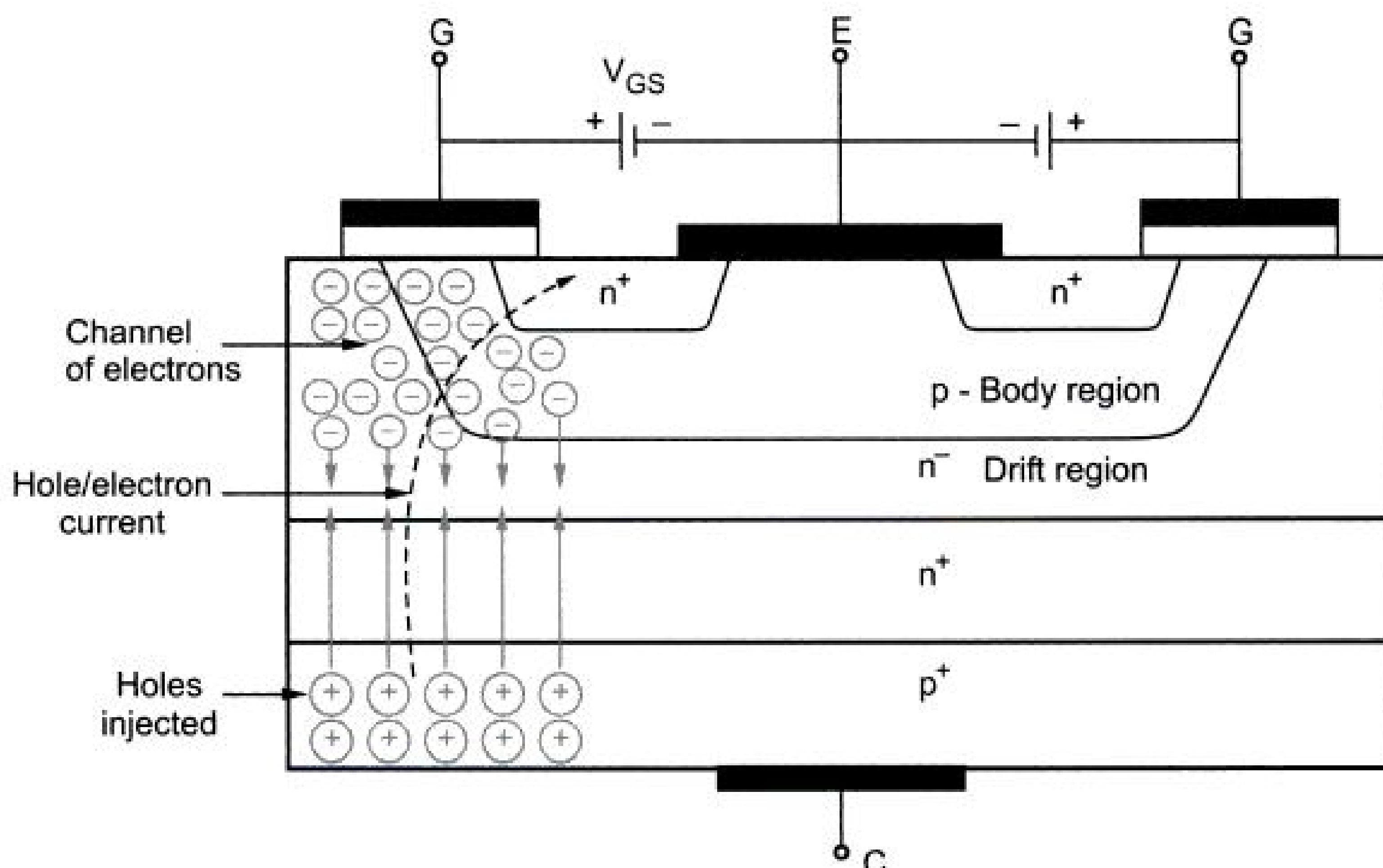


Fig. 1.4.3 A positive gate to source voltage initiates MOSFET action

Copyrighted material

hole/electron current starts flowing from collector to emitter. When holes enter p-type body region, they attract more electrons from n^+ layer. This action is exactly similar to MOSFET.

Difference in operation Compared to MOSFET - *Conductivity Modulation*

Now let us see how p^+ injecting layer makes the operation different than MOSFET. Fig. 1.4.4 shows the structure of IGBT showing how internal MOSFETs and transistors are formed. The MOSFET is formed with input gate, emitter as source and n^- drift region as drain. The two transistors T_1 and T_2 are formed as shown. The holes injected by the p^+ injecting layer go to the n^- drift region. This n^- drift region is base of T_1 and collector of T_2. The holes in the n^- drift region further go to the p-type body region, which is connected to the emitter. The electrons from n^+ region (which is emitter) pass through the transistor T_2 and further in the n^- drift region. Thus holes and electrons are injected in large amounts in n^- drift region. This reduces the resistance of the n^- drift region. This is called *conductivity modulation* of n^- drift region. Note that such conductivity modulation does not exist in MOSFET.

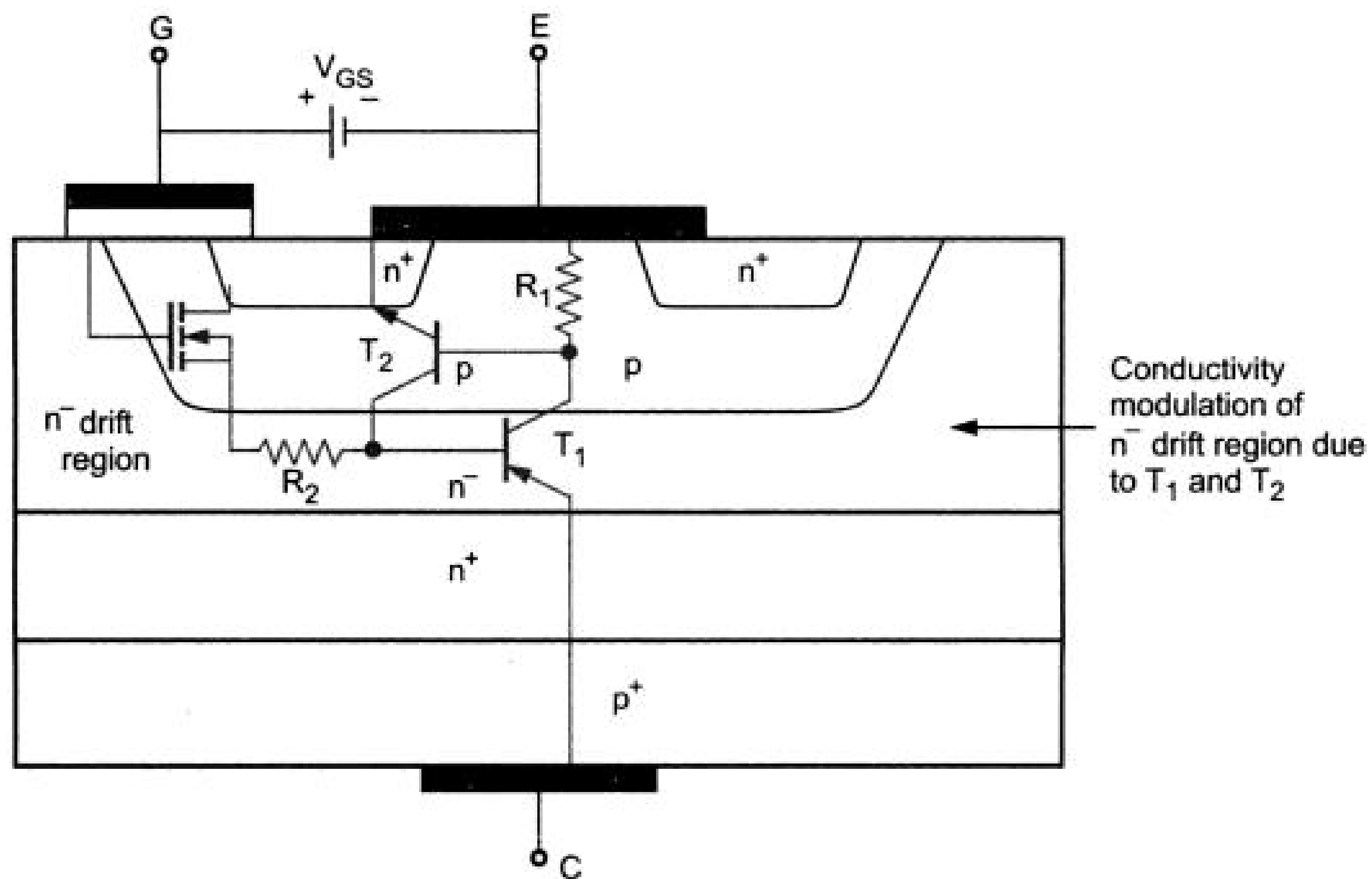


Fig. 1.4.4 Structure of IGBT

How on-state loss is reduced?

The connection of T_1 and T_2 is such that large amount of hole/electrons are injected in n^- drift region. The action of T_1 and T_2 is like SCR which is regenerative. The gate serves as trigger for T_1 through internally formed MOSFET. Fig. 1.4.5 shows the equivalent circuit. In this Fig. 1.4.5 observe that when gate is applied ($V_{GS} > V_{GS(th)}$), the internal equivalent MOSFET turns on. This gives base drive to T_1. Hence T_1 starts conducting. The collector of

Copyrighted material

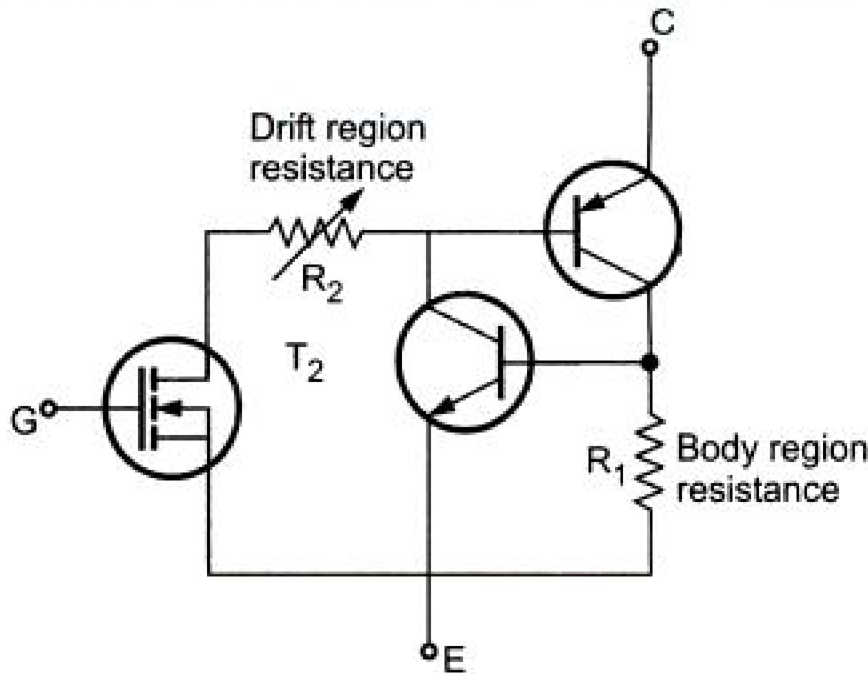


Fig. 1.4.5 Equivalent circuit of IGBT

T_1 is base of T_2. Therefore T_2 also turns on. The collector of T_2 is base of T_1. Thus the regenerative loop begins and large number of carriers are injected in n^- drift region. This reduces the on-state loss of the IGBT just like BJT. This happens due to conductivity modulation of n^- drift region.

When the gate drive is removed, the IGBT should turn-off. When gate is removed, the induced channel will be vanished and internal equivalent MOSFET will turn-off. Hence T_1 will turn-off if T_2 turns-off. T_2 will turn-off if the p-type body region resistance R_1 is very very small. Under such situation, its base and emitter will be virtually shorted. Hence T_2 turns-off. Therefore T_1 will also turn-off. Hence structure of IGBT is organized such that body region resistance (R_1) is very very small.

If R_1 is very very small, then T_2 will never conduct and the equivalent circuit of IGBT will be as shown in Fig. 1.4.6. IGBTs are thus different than MOSFETs because of conduction of current from collector to emitter. For MOSFETs, on state losses are high since resistance of drift region remains same. But in IGBTs, resistance of drift region reduces when gate drive is applied. This resistance reduces because of p^+ injecting region. Hence, on-state loss of IGBT is very small.

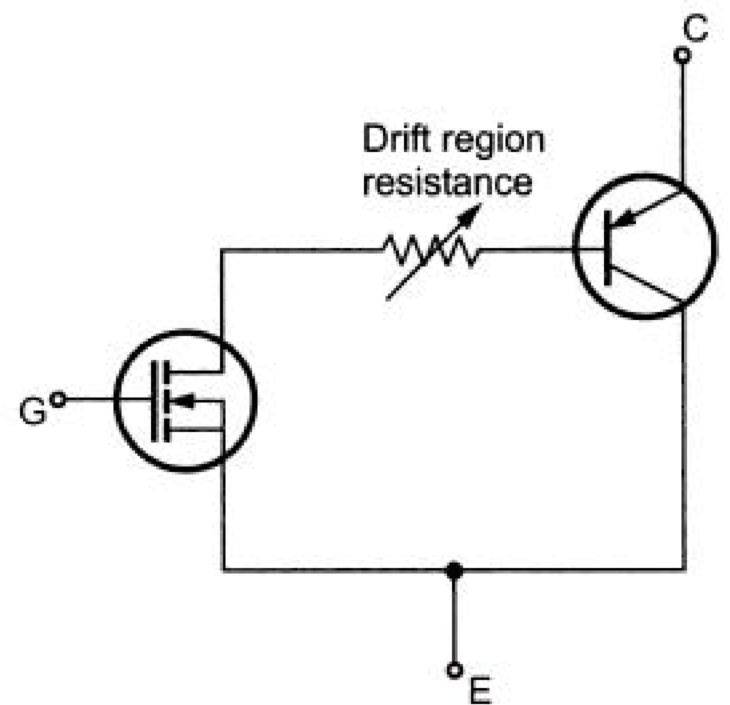


Fig. 1.4.6 Simplified equivalent circuit of IGBT

1.4.1.4 Latchup in IGBT

Answer following question after reading this topic.

1. *Explain, with the help of equivalent circuits, causes of latchups in IGBT and how to avoid it ?*
Marks [3], Dec.-2006; Marks [6], Dec.-2007

Most likely and **asked in** previous University Exam

- Latchup means IGBT remains in ON condition even if gate drive is removed.
- **Causes of latchup :** The current in p-type body region flows vertically as well as laterally. In equivalent circuit of Fig. 1.4.5 observe that the lateral component of

Copyrighted material

current flows through the body region resistance R_1. Therefore the drop across this body region resistance is sufficient to turn-on npn transistor T_2. Therefore pnp transistor T_1 is also turned on and regeneration takes place. Under this situation gate has no control over the current flow. Thus IGBT remains in ON condition even if gate drive is removed.

- **To avoid latchups :**

i) Efforts are made to reduce the body resistance R_1. This can be achieved by using special geometries for the structure of IGBT.

ii) The circuit should be designed in such a way that maximum specified current should not be exceeded.

iii) Latchups can also be avoided by increasing the turn-off time and controlling h_{FE} of the pnp transistor.

1.4.1.5 Body-Source-Short and its Reason

Answer following question after reading this topic.

1. *Explain the reason for the body-source-short in the IGBT structure.* **Marks [2] May-2006**

Most likely and **asked in** previous University Exam

What is body-source-short?

In the structure of IGBT observe that the source (or emitter 'E') is connected to p-type body region as well as n^+ region. This means p-type body region is shorted to source (or emitter 'E').

Reason

In Fig. 1.4.4 observe that various layers of IGBT form internal parasitic thyristor i.e. ($p^+ - n^+ n^- - p - n^+$). The body-source-short avoids possible turn-on of this parasitic thyristor. The base-emitter (i.e p-type body region and n^+ region) of transistor T_2 are shorted due to body-source-short. Hence it does not conduct. It also helps in avoiding latchup in IGBT.

Copyrighted material

1.4.2 Safe Operating Area (SOA) of IGBT

Answer following question after reading this topic.

1. *Draw the forward biased and reverse biased SOA of an IGBT.*
   Marks [4], May-2003

Most likely and **asked in** previous University Exam

1.4.2.1 Forward Biased SOA (FBSOA)

Answer following question after reading this topic.

1. *Draw the forward biased SOA of an IGBT.*
   Marks [2], Dec.-2004, May-2006

Most likely and **asked in** previous University Exam

- The FBSOA is the square for turn-on times less than 1 msec.
- For reduced switching times FBSOA is limited by maximum junction temperature.

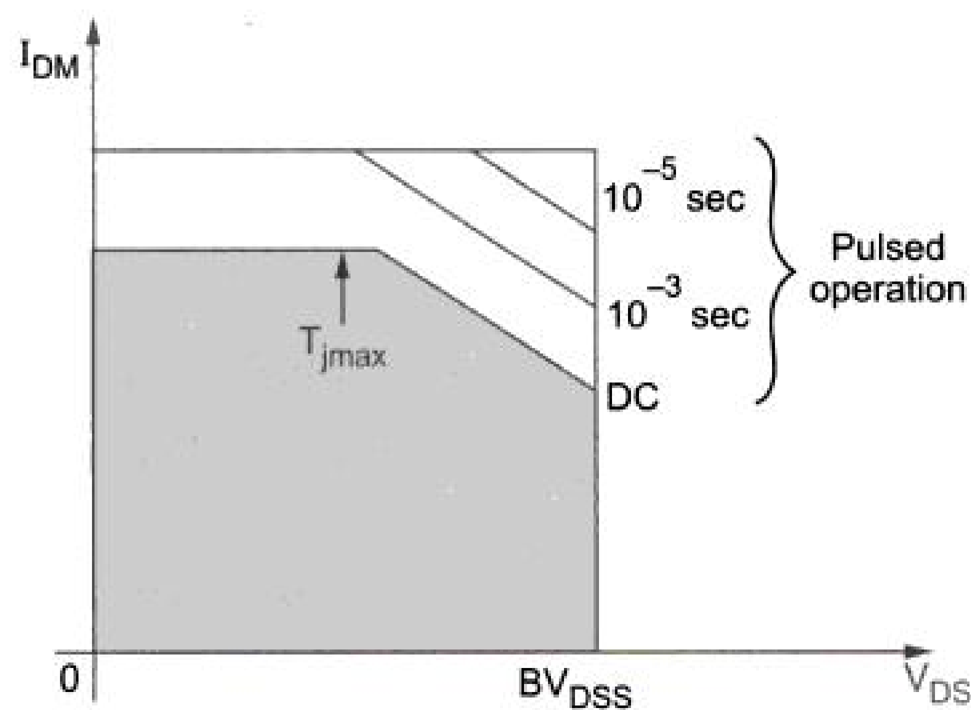


Fig. 1.4.7 FBSOA of IGBT

1.4.2.2 Reverse Biased SOA (RBSOA)

- The RBSOA depends upon the reapplied rate of change of drain-source voltage.
- Observe that the RBSOA reduces as dV_{DS} / dt increases.
- The reduction in RBSOA is necessary to avoid latchups.

Copyrighted material

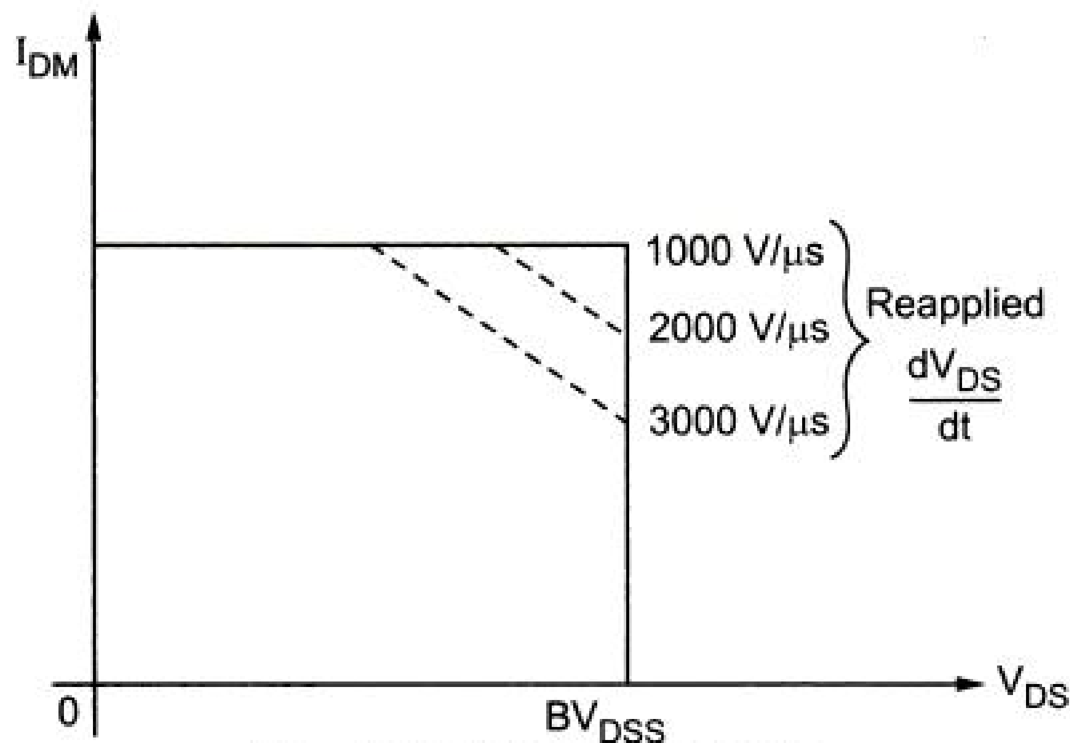


Fig. 1.4.8 RBSOA of IGBT

1.4.2.3 Superiority of SOA of IGBT and its Comparison with SOA of MOSFET and BJT

Answer following questions after reading this topic.

1. *What is the principle difference between the forward biased SOAs of i) IGBT and BJT ii) IGBT and power MOSFET.*
Marks [4], May-2003
2. *Explain how SOA of an IGBT is superior to that of power BJT.*
Marks [2], Dec.-2004, May-2006

Most likely and **asked in** previous University Exam

- The SOA of IGBT is square for short switching times.
- The RBSOA of IGBT indicates significantly higher values of reapplied dv/dt.
- The SOA of IGBT is wider compared to that of BJT.
- As switching frequency increases, the SOA of BJT reduces considerably.
- The FBSOA of MOSFET and IGBT are similar for short switching times (i.e. less than 1 ms).
- The FBSOA of MOSFET and IGBT do not show second breakdown, since it is present only in BJTs.
- For longer switching times, the FBSOA of BJT, MOSFET and IGBT are restricted by maximum junction temperature.
- The RBSOA and FBSOA are identical in case of MOSFETs. But RBSOA is larger in case of BJT and it is smaller in case of IGBT compared to their corresponding FBSOA.

Copyrighted material

1.4.3 Steady State (V-I) and Transfer Characteristics of IGBT

Answer following question after reading this topic.

1. *Draw the output (V - I) and transfer characteristics of an IGBT.*
   Marks [2], May-2001, May-2006, Marks [4], Dec.-2004

Most likely and **asked in** previous University Exam

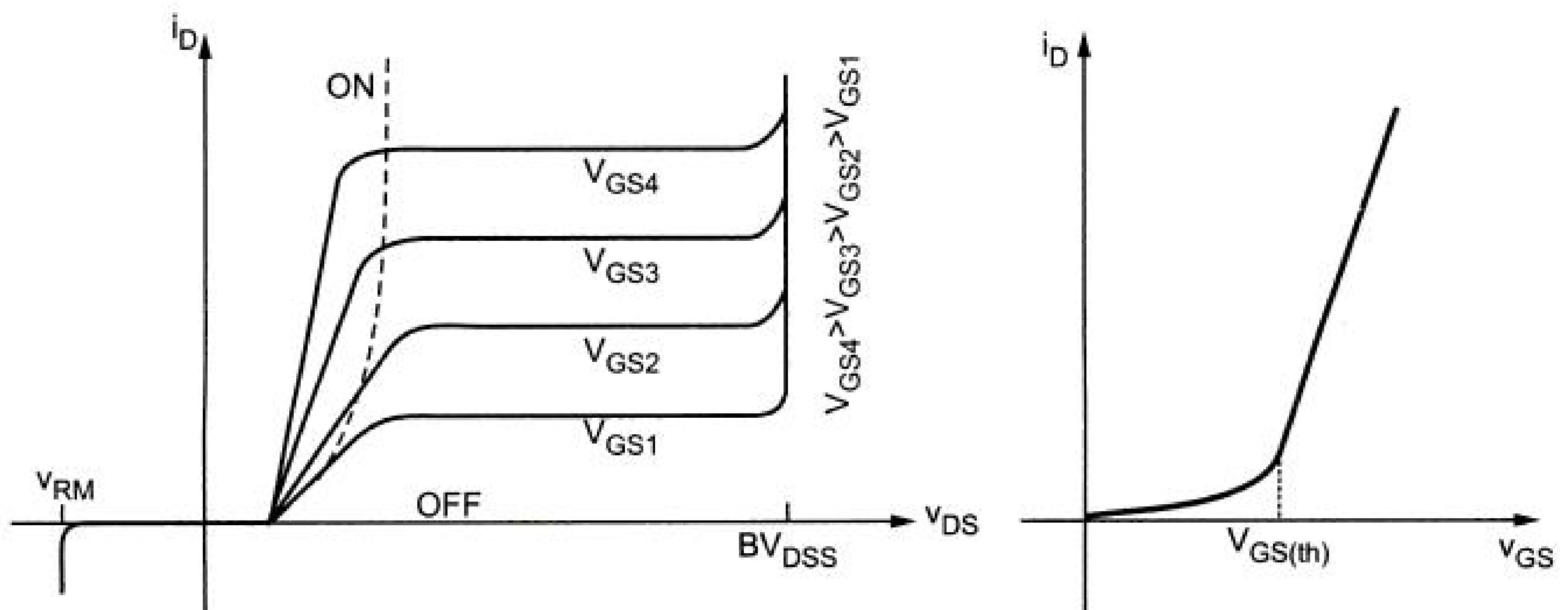
1.4.3.1 Steady State (V - I) or Output Characteristics

Answer following questions after reading this topic.

1. *Draw the V - I characteristics of an IGBT.* **Marks [2], Dec.-2006**
2. Explain the characteristics of an IGBT.

Most likely and **asked in** previous University Exam

Fig. 1.4.9 (a) shows the V-I characteristics of n-channel IGBT. Sometime the collector is also called drain and emitter is also called source. The characteristics are plotted for drain (collector) current i_D with respect to drain source (collector emitter) voltage V_{DS}. The characteristics are plotted for different values of gate to source (V_{GS}) voltages. When the gate to source voltage is greater than the threshold voltage $V_{GS(th)}$, then IGBT turns-on. The IGBT is off when V_{GS} is less than $V_{GS(th)}$. Fig. 1.4.9 shows the 'on' and 'off' regions of IGBT. The BV_{DSS} is the breakdown drain to source voltage when gate is open circuitted. The IGBT is the popular device now-a-days. IGBT has simplest drive circuit and it has low on-state losses.



(a) V-I characteristics of n-channel IGBT (b) Transfer characteristic

Fig. 1.4.9

Copyrighted material

1.4.3.2 Transfer Characteristics

The drain current versus gate-source voltage is called transfer characteristic. It is shown in Fig. 1.4.9 (b). This characteristic relates variation in output current with respect to variation in input voltage. Transfer characteristics are reasonably linear over most of the range of drain currents. The characteristics becomes nonlinear when gate to source voltage approaches $V_{GS(th)}$. When the gate to source voltage is less than $V_{GS(th)}$ i.e. threshold value, the IGBT goes in off state.

1.4.4 Switching Characteristics of IGBT

Fig. 1.4.10 shows the switching characteristics of IGBT. The gate to source voltage is normally negative. This voltage is made positive to turn-on the IGBT. When $V_{GS} > V_{GS(th)}$, the collector current starts increasing. Turn-on delay, $t_{d(on)}$ is the delay when gate drive is applied and i_C starts increasing. When i_C increases to its full value, collector emitter voltage starts falling. 't_{ri}' is the rise time of collector and t_{fv} is the fall time of voltage. Thus, turn-on time of IGBT is,

$$t_{on} = t_{d(on)} + t_{ri} + t_{fv}$$

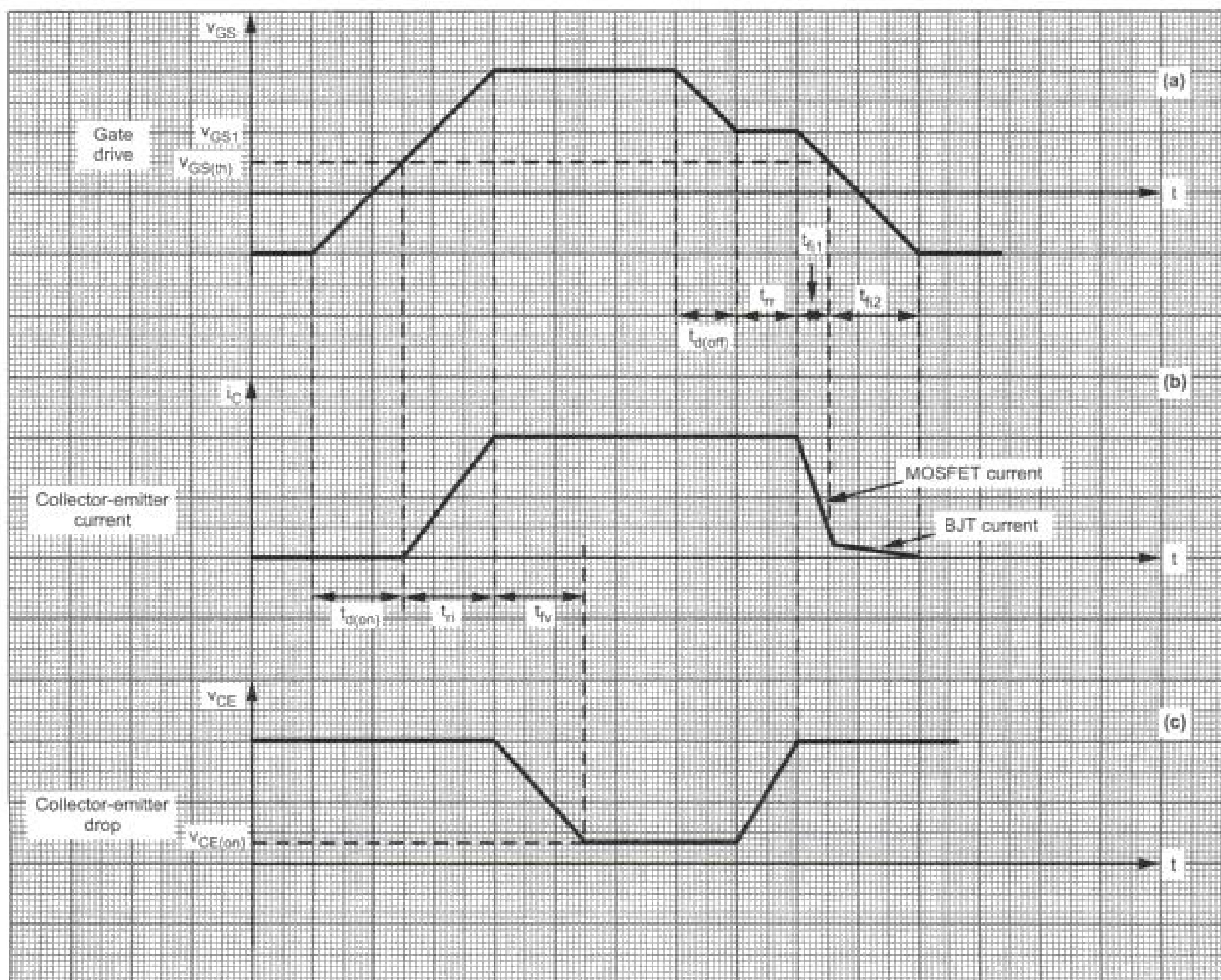


Fig. 1.4.10 Switching characteristics of IGBT

Copyrighted material

The turn-off of the IGBT is initiated by reducing the gate voltage. When gate voltage falls to the value equal to v_{GS1}, v_{CE} starts rising. v_{GS1} is the voltage where IGBT comes out of saturation. Turn-off delay, $t_{d(off)}$ is the delay time when gate voltage is reduced and v_{CE} starts increasing. When v_{CE} reaches to supply voltage, i_C starts reducing. i_C reduces fast till v_{GS} reaches to $v_{GS(th)}$. This fast decay in i_C is basically due to internal MOSFET. Then v_{GS} goes to zero and becomes negative. But i_C keeps on flowing for sometime. This is internal BJT current. This current flows due to stored carriers in the drift region. Hence, turn-off time of IGBT is higher than IGBT. The turn-off time of IGBT will be,

$$t_{off} = t_{d(off)} + t_{rv} + t_{fi_1} + t_{fi_2}$$

Here, t_{rv} is voltage rise time.

t_{fi_1} is MOSFET current fall time.

t_{fi_2} is BJT current fall time.

1.4.5 Merits, Demerits and Applications of IGBT

1.4.5.1 Merits of IGBT

Answer following question after reading this topic.

1. *What are the advantages of IGBT over power MOSFET and power BJT ?* **Marks[4], May-2000, Dec.-2000; Marks[6], Dec.-2001; Marks[5], May-2002**

Most likely and **asked in** previous University Exam

(i) Voltage controlled device. Hence drive circuit is very simple.

(ii) On-state losses are reduced compared to BJT, MOSFET and SCR.

(iii) Switching frequencies are higher than thyristors.

(iv) No commutation circuits are required as compared to SCR.

(v) Gate have full control over the operation of IGBT.

(vi) IGBTs have approximately flat temperature coefficient.

(vii) The drive of IGBT is simple and driving current requirement is also very small as compared to BJT, since there is no direct current flow in the gate.

(viii) The voltage and current ratings of the IGBTs are better compared to MOSFETs.

1.4.5.2 Demerits of IGBT

(i) IGBTs have static charge problems.

(ii) IGBTs are costlier than BJTs and MOSFETs.

Copyrighted material