CHAPTER 9

RESONANT CONVERTERS: ZERO-VOLTAGE AND/OR ZERO-CURRENT SWITCHINGS

9-1 INTRODUCTION

In all the pulse-width-modulated dc-to-dc and dc-to-ac converter topologies discussed in Chapters 7 and 8, the controllable switches are operated in a switch mode where they are required to turn on and turn off the entire load current during each switching. In this switch-mode operation, as explained further in Section 9-1-1, the switches are subjected to high switching stresses and high switching power loss that increases linearly with the switching frequency of the PWM. Another significant drawback of the switch-mode operation is the EMI produced due to large di/dt and dv/dt caused by a switch-mode operation.

These shortcomings of switch-mode converters are exacerbated if the switching frequency is increased in order to reduce the converter size and weight and hence to increase the power density. Therefore, to realize high switching frequencies in converters, the aforementioned shortcomings are minimized if each switch in a converter changes its status (from on to off or vice versa) when the voltage across it and/or the current through it is zero at the switching instant. The converter topologies and the switching strategies, which result in zero-voltage and/or zero-current switchings, are discussed in this chapter. Since most of these topologies (but not all) require some form of LC resonance, these are broadly classified as "resonant converters."

9-1-1 SWITCH-MODE INDUCTIVE CURRENT SWITCHING

This topic was briefly reviewed in Chapter 2. To illustrate further the problems associated with switch-mode operation, consider one of the legs of a full-bridge dc–dc converter or a dc-to-ac inverter (single phase or three phase), as shown in Fig. 9-1. The output current can be in either direction and can be assumed to have a constant magnitude I_o due to the load inductance, during the very brief switching interval. The linearized voltage and current waveforms, for example, for the lower switch T_- are shown in Fig. 9-2*a*.

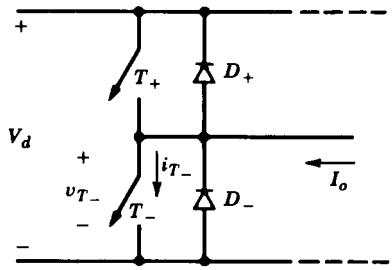


Figure 9-1 One inverter leg.

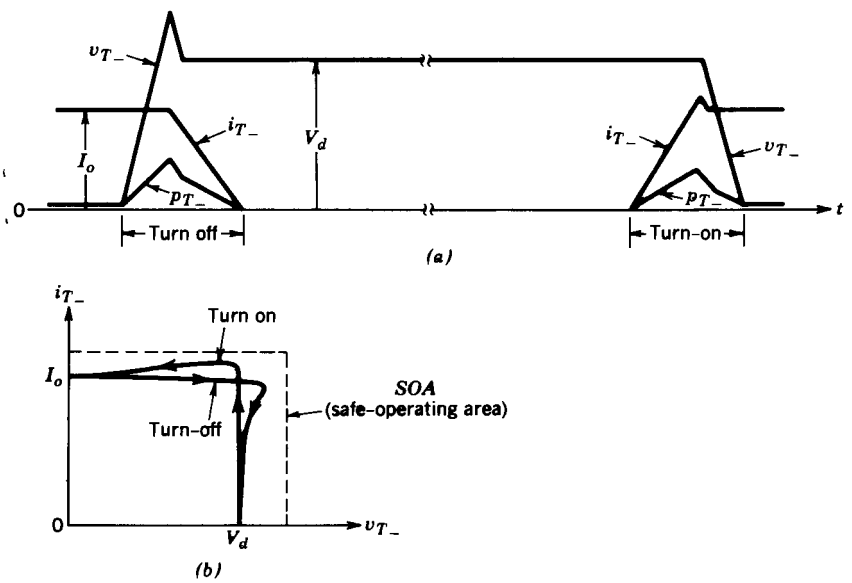


Figure 9-2 Switch-mode inductive current switchings.

Initially, I_o is assumed to be flowing through T_-. If a control signal is applied to turn T_- off, the switch voltage v_{T_-} increases to V_d (it overshoots V_d due to stray inductances), and then the switch current i_{T_-} decays to zero. After the turn-off of T_-, I_o flows through D_+. The power loss P_{T-} ($=v_{T-}\cdot i_{T-}$) in the switch during turn-off is shown in Fig. 9-2*a*.

Now consider the turn-on of T_-. Prior to the turn-on of T_-, I_o is flowing through D_+. When the switch control signal is applied to turn T_- on, i_{T_-} increases to I_o plus the peak-reverse-recovery current of the diode D_+, as shown in Fig. 9-2*a*. Subsequently, the diode recovers and the switch voltage v_{T-} and i_{T-} results in a switching power loss in T_- during turn-on.

The average value of the switching loss P_{T-}, being proportional to the switching frequency, limits how high the switching frequency can be pushed without significantly degrading the system efficiency. With the availability of fast switches (with the switching times as low as a few tens of nanoseconds), the present limit seems to be up to approximately 500 kHz with a reasonable energy efficiency.

Another significant disadvantage of the switch-mode operation is that it results in large *di/dt* and *dv/dt* due to fast switching transitions required to keep the switching losses in the switch as low as possible. Diodes with poor reverse-recovery characteristics significantly add to this phenomenon, which produces EMI.

Switch-mode inductive current switching results in switching loci in the v_T–i_T plane, as shown in Fig. 9-2*b*. Because a large switch voltage and a large switch current occur

simultaneously, the switch must be capable of withstanding high switching stresses, with a safe operating area (SOA), as shown by the dashed lines. This requirement to be able to withstand such large stresses results in undesirable design compromises in other characteristics of the power semiconductor devices.

9-1-2 ZERO-VOLTAGE AND ZERO-CURRENT SWITCHINGS

Switching frequencies in the megahertz range, even tens of megahertz, are being contemplated to reduce the size and the weight of transformers and filter components and, hence, to reduce the cost as well as the size and the weight of power electronics converters. Realistically, the switching frequencies can be increased to such high values only if the problems of switch stresses, switching losses, and the EMI associated with the switch-mode converters can be overcome.

The switch stresses, as discussed in later chapters in this book, can be reduced by connecting simple dissipative snubber circuits (consisting of diodes and passive components) in series and parallel with the switches in the switch-mode converters. Such snubber circuits are shown in Fig. 9-3*a*, and the switching loci that result in reduced switch stresses are shown in Fig. 9-3*b*. However, these dissipative snubbers shift the switching power loss from the switch to the snubber circuit and therefore do not provide a reduction in the overall switching power loss.

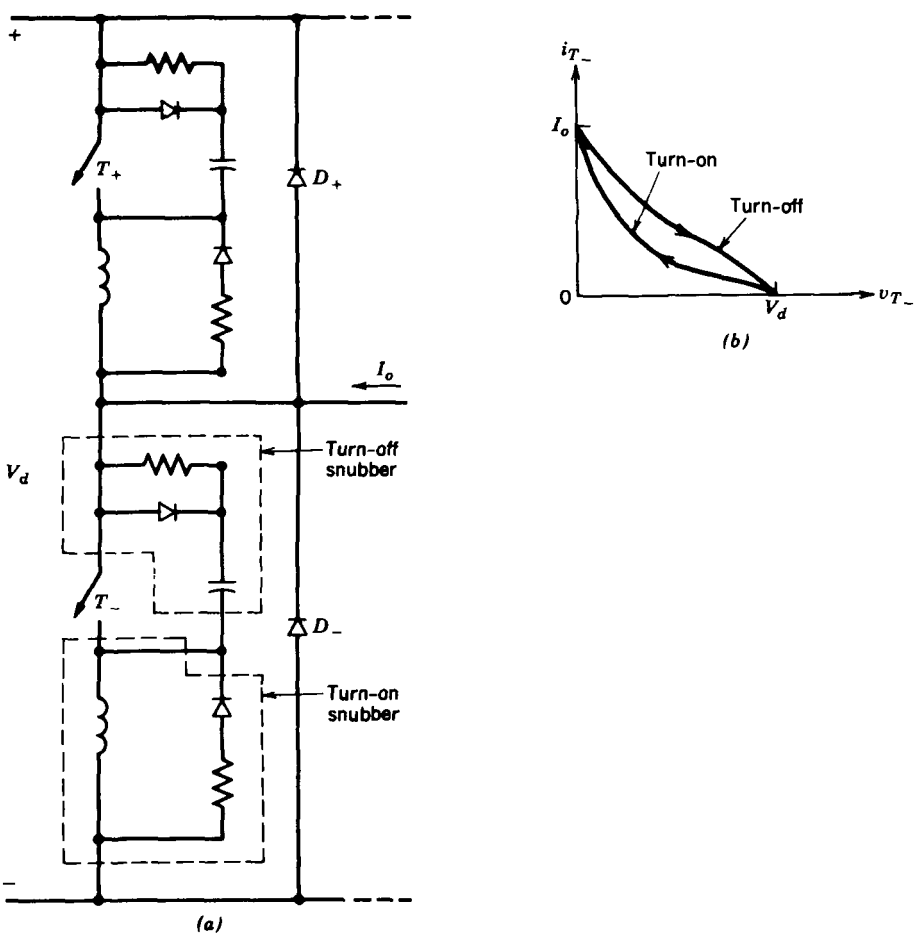


Figure 9-3 Dissipative snubbers: (*a*) snubber circuits; (*b*) switching loci with snubbers.

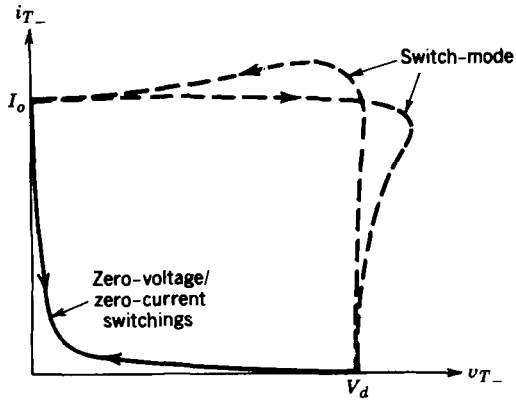


Figure 9-4 Zero-voltage-/zero-current-switching loci.

In contrast to dissipative snubbers in switch-mode converters, the combination of proper converter topologies and switching strategies can overcome the problems of switching stresses, switching power losses, and the EMI by turning on and turning off each of the converter switches when either the switch voltage or the switch current is zero. Ideally, both the switch voltage and current should be zero when the switching transition occurs.

As a brief introduction, once again consider the one-leg inverter of Fig. 9-1. If both the turn-on and turn-off switchings occur under a zero-voltage and/or a zero-current condition, then the switching loci are shown in Fig. 9-4, where the switching loci in the switch mode are shown (by dashed curves) for comparison purposes. Such switching loci, without dissipative snubbers, reduce switch stresses, switching power losses, and the EMI.

9-2 CLASSIFICATION OF RESONANT CONVERTERS

The resonant converters are defined here as the combination of converter topologies and switching strategies that result in zero-voltage and/or zero-current switchings. One way to categories these converters is as follows:

1. Load-resonant converters
2. Resonant-switch converters
3. Resonant-dc-link converters
4. High-frequency-link integral-half-cycle converters

These classifications are explained further.

9-2-1 LOAD-RESONANT CONVERTERS

These converters consist of an *LC* resonant tank circuit. Oscillating voltage and current, due to *LC* resonance in the tank are applied to the load, and the converter switches can be switched at zero voltage and/or zero current. Either a series *LC* or a parallel *LC* circuit can be used. In these converter circuits, the power flow to the load is controlled by the resonant tank impedance, which in turn is controlled by the switching frequency f_s in comparison to the resonant frequency f_0 of the tank. These dc-to-dc and dc-to-ac converters can be subclassified as follows:

1. Voltage-source series-resonant converters
   (a) Series-loaded resonant (SLR) converters
   (b) Parallel-loaded resonant (PLR) converters
   (c) Hybrid-resonant converters
2. Current-source parallel-resonant converters
3. Class E and subclass E resonant converters

9-2-2 RESONANT-SWITCH CONVERTERS

In certain switch-mode converter topologies, an *LC* resonance can be utilized primarily to shape the switch voltage and current to provide zero-voltage and/or zero-current switchings. In such resonant-switch converters, during one switching-frequency time period, there are resonant as well as nonresonant operating intervals. Therefore, these converters in the literature have also been termed quasi-resonant converters. They can be subclassified as follows:

1. Resonant-switch dc–dc converters
   (a) Zero-current-switching (ZCS) converters
   (b) Zero-voltage-switching (ZVS) converters
2. Zero-voltage-switching, clamped-voltage (ZVS-CV) converters, which are also referred to as pseudo-resonant converters and resonant-transition converters, respectively in references 34 and 31.

9-2-3 RESONANT-dc-LINK CONVERTERS

In the conventional switch-mode PWM dc-to-ac inverters, the input V_d to the inverter is a fixed-magnitude dc, and the sinusoidal output (single phase or three phase) is obtained by switch-mode PWM switchings. However, in the resonant-dc-link converters, the input voltage is made to oscillate around V_d by means of an *LC* resonance so that the input voltage remains zero for a finite duration during which the status of the inverter switches can be changed, thus resulting in zero-voltage switchings.

9-2-4 HIGH-FREQUENCY-LINK INTEGRAL-HALF-CYCLE CONVERTERS

If the input to a single-phase or three-phase inverter is a high-frequency sinusoidal ac, then by using bidirectional switches it is possible to synthesize a low-frequency ac of adjustable magnitude and frequency or an adjustable-magnitude dc, where the switches are turned on and off at the zero crossings of the input voltage.

9-3 BASIC RESONANT CIRCUIT CONCEPTS

Some basic configurations encountered in the resonant converters discussed in this chapter are analyzed in a generic fashion. Appropriate assumptions are made to keep the analysis simple.

The initial conditions are indicated by uppercase letters, subscript 0, and square brackets, for example, $[V_{c0}]$ and $[I_{c0}]$.

9-3-1 SERIES-RESONANT CIRCUITS

9-3-1-1 Undamped Series-Resonant Circuit

Figure 9-5*a* shows an undamped series-resonant circuit where the input voltage is V_d at time t_0. The initial conditions are I_{L0} and V_{c0}. With the inductor current i_L and the capacitor voltage v_c as the state variables, the circuit equations are

$$L_r\frac{di_L}{dt} + v_c = V_d \tag{9-1}$$

and

$$C_r\frac{dv_c}{dt} = i_L \tag{9-2}$$

The solution of this set of equations for $t \geq t_0$ is as follows:

$$i_L(t) = I_{L0}\cos\omega_0(t - t_0) + \frac{V_d - V_{c0}}{Z_o}\sin\omega_0(t - t_0) \tag{9-3}$$

and

$$v_c(t) = V_d - (V_d - V_{c0})\cos\omega_0(t - t_0) + Z_0 I_{L0}\sin\omega_0(t - t_0) \tag{9-4}$$

where

$$\text{Angular resonance frequency} = \omega_0 = 2\pi f_0 = \frac{1}{\sqrt{L_r C_r}} \tag{9-5}$$

and

$$\text{Characteristic impedance} = Z_0 = \sqrt{\frac{L_r}{C_r}} \quad \Omega \tag{9-6}$$

To plot normalized v_c and i_L, the following base quantities are chosen:

$$V_{\text{base}} = V_d \tag{9-7}$$

and

$$I_{\text{base}} = \frac{V_d}{Z_0} \tag{9-8}$$

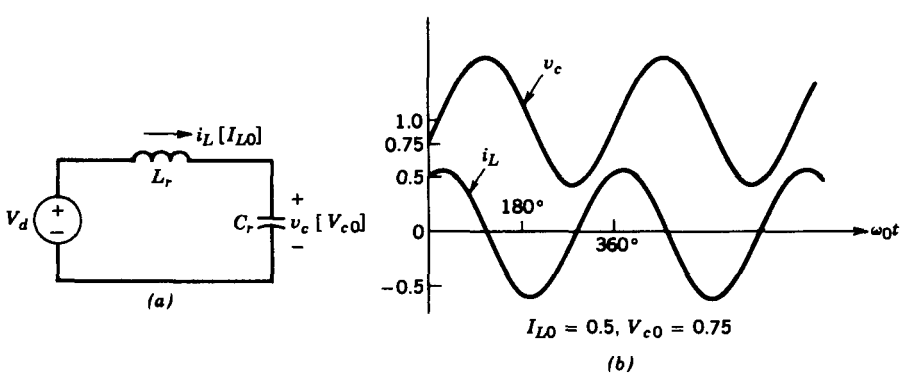


Figure 9-5 Undamped series-resonant circuit; i_L and v_c are normalized: (*a*) circuit; (*b*) waveforms with $I_{L0} = 0.5$, $V_{c0} = 0.75$.

As an example, the normalized i_L and v_c are plotted in Fig. 9-5*b* for $I_{L0} = 0.5$ and $V_{c0} = 0.75$.

9-3-1-2 Series-Resonant Circuit with a Capacitor-Parallel Load

Figure 9-6*a* shows a series-resonant circuit, where the capacitor is in parallel with a current I_o, which represents the load. In this circuit, V_d and I_o are dc quantities. The initial conditions are I_{L0} and V_{c0} at the initial time t_0. Therefore

$$v_c = V_d - L_r \frac{di_L}{dt} \tag{9-9}$$

and

$$i_L - i_c = I_o \tag{9-10}$$

By differentiating Eq. 9-9

$$i_c = C_r \frac{dv_c}{dt} = -L_r C_r \frac{d^2 i_L}{dt^2} \tag{9-11}$$

Substituting i_c from Eq. 9-11 into Eq. 9-10 yields

$$\frac{d^2 i_L}{dt^2} + \omega_0^2 i_L = \omega_0^2 I_o \tag{9-12}$$

where ω_0 is the same as in Eq. 9-5. Solution of these equations for $t \geq t_0$ is as follows:

$$i_L(t) = I_o + (I_{L0} - I_o)\cos \omega_0(t - t_0) + \frac{V_d - V_{c0}}{Z_0}\sin \omega_0(t - t_0) \tag{9-13}$$

and

$$v_c(t) = V_d - (V_d - V_{c0})\cos \omega_0(t - t_0) + Z_0(I_{L0} - I_o)\sin \omega_0(t - t_0) \tag{9-14}$$

where ω_0 is the angular resonant frequency as defined in Eq. 9-5 and Z_0 is the characteristic impedance defined in Eq. 9-6.

In a special case with $V_{c0} = 0$ and $I_{L0} = I_o$,

$$i_L(t) = I_o + \frac{V_d}{Z_0}\sin \omega_0(t - t_0) \tag{9-15}$$

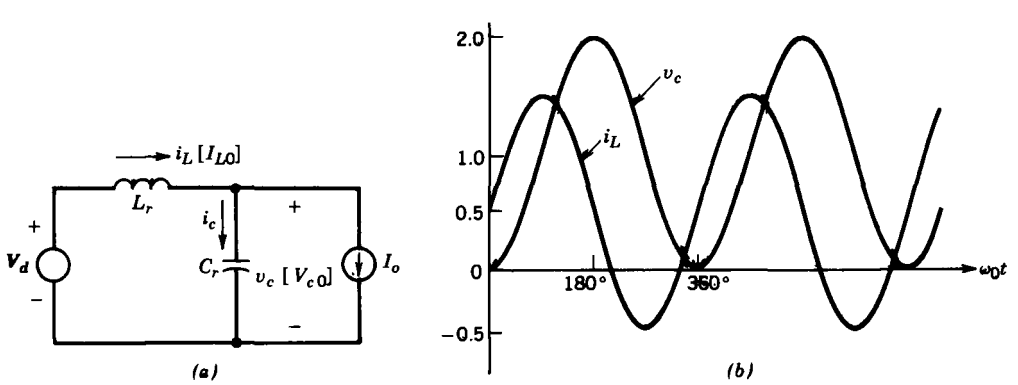


Figure 9-6 Series-resonant circuit with capacitor-parallel load (i_L and v_c are normalized): (*a*) circuit; (*b*) $V_{c0} = 0$, $I_{L0} = I_o = 0.5$.

and

$$v_c(t) = V_d[1 - \cos \omega_0(t - t_0)] \tag{9-16}$$

For this special case, Fig. 9-6*b* shows the plot of i_L and v_c, which are normalized by using Eqs. 9-7 and 9-8, respectively, and $I_{LO} = I_o = 0.5$ per unit.

9-3-1-3 Frequency Characteristics of a Series-Resonant Circuit

It is informative to obtain the frequency characteristics of the series-resonant circuit of Fig. 9-7*a*. The resonance frequency ω_0 and the characteristic impedance Z_0 are defined by Eqs. 9-5 and 9-6, respectively. In the presence of a load resistance R, another quantity called the quality factor Q is defined as

$$Q = \frac{\omega_0 L_r}{R} = \frac{1}{\omega_0 C_r R} = \frac{Z_0}{R} \tag{9-17}$$

Figure 9-7*b* shows the magnitude Z_s of the circuit impedance as a function of frequency with Q as a parameter, keeping R constant. It shows that Z_s is a pure resistance equal to R at $\omega_s = \omega_0$ and is very sensitive to frequency deviation from ω_0 at higher values of Q.

Figure 9-7*c* shows the current phase angle θ $(=\theta_i - \theta_v)$ as a function of frequency. The current leads at frequencies below ω_0 $(\omega_s < \omega_0)$, where the capacitor impedance dominates over inductor impedance. At frequencies above ω_0 $(\omega_s > \omega_0)$, the inductor impedance dominates over the capacitor impedance and the current lags the voltage, with the current phase angle θ approaching $-90°$.

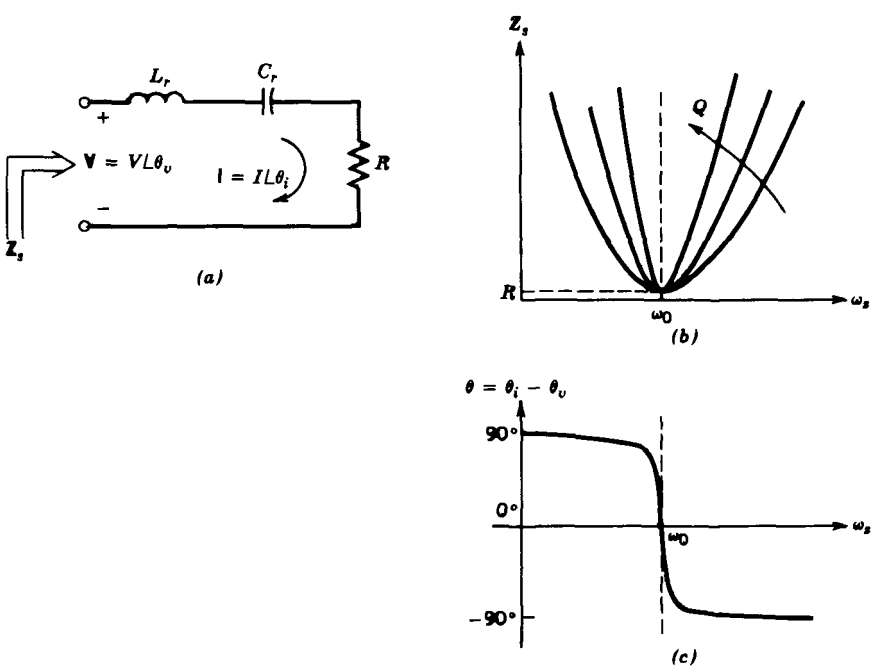


Figure 9-7 Frequency characteristics of a series-resonant circuit.

9-3-2 PARALLEL-RESONANT CIRCUITS

9-3-2-1 Undamped Parallel-Resonant Circuit

Figure 9-8*a* shows an undamped parallel-resonant circuit supplied by a dc current I_d. The initial conditions at time $t = t_0$ are I_{L0} and V_{c0}. With the inductor current i_L and the capacitor voltage v_c as the state variables, the circuit equations are

$$i_L + C_r\frac{dv_c}{dt} = I_d \tag{9-18}$$

and

$$v_c = L_r\frac{di_L}{dt} \tag{9-19}$$

The solution of the foregoing sets of equations for $t \geq t_0$ is as follows:

$$i_L(t) = I_d + (I_{L0} - I_d)\cos\,\omega_0(t - t_0) + \frac{V_{c0}}{Z_0}\sin\,\omega_0(t - t_0) \tag{9-20}$$

and

$$v_c(t) = Z_0(I_d - I_{L0})\sin\,\omega_0(t - t_0) + V_{c0}\cos\,\omega_0(t - t_0) \tag{9-21}$$

where

$$\omega_0 = \frac{1}{\sqrt{L_rC_r}} \tag{9-22}$$

and

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \tag{9-23}$$

9-3-2-2 Frequency Characteristics of Parallel-Resonant Circuit

It is informative to obtain the frequency characteristics of the parallel-resonant circuit of Fig. 9-9*a*. The reasonance frequency ω_0 and Z_0 are as defined by Eqs. 9-22 and 9-23, respectively. In the presence of a load resistor R, another quantity called the quality factor Q is defined, where

$$Q = \omega_0RC_r = \frac{R}{\omega_0L_r} = \frac{R}{Z_0} \tag{9-24}$$

Figure 9-9*b* shows the magnitude Z_p of the circuit impedance as a function of frequency with Q as a parameter, keeping R constant.

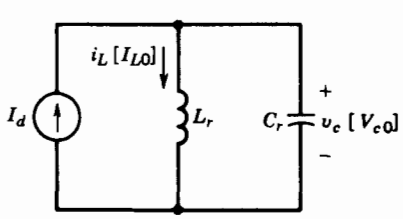


Figure 9-8 Undamped parallel-resonant circuit.

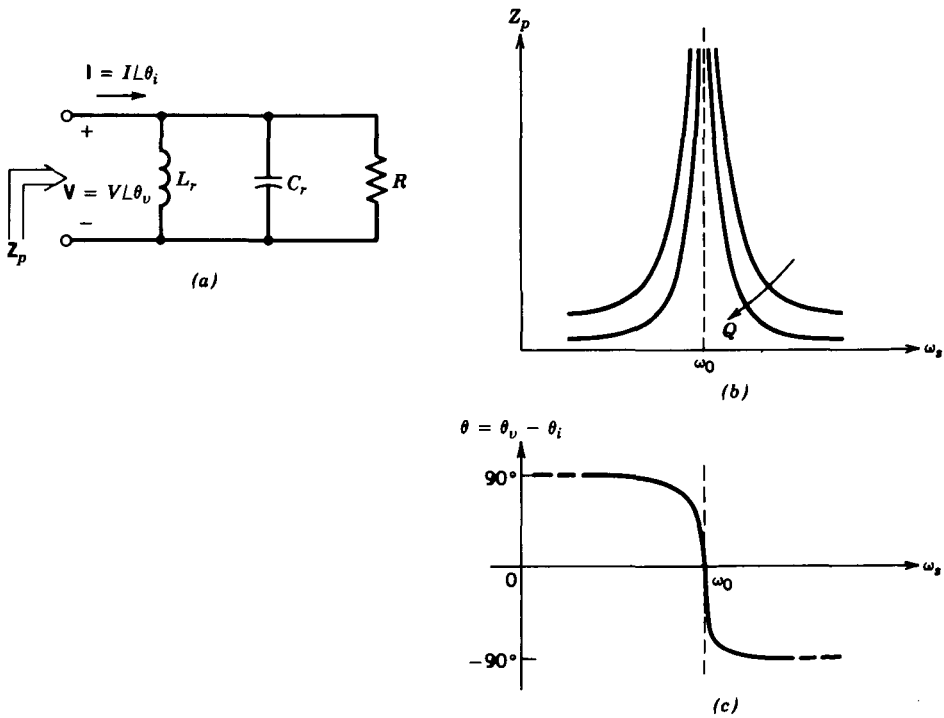


Figure 9-9 Frequency characteristics of a parallel-resonant circuit.

Figure 9-9*c* shows the voltage phase angle θ ($=\theta_v - \theta_i$) as a function of frequency. The voltage leads the current at frequencies below ω_0 ($\omega_s < \omega_0$), where the inductor impedance is lower than the capacitor impedance, and hence the inductor current dominates. At frequencies above ω_0 ($\omega_s > \omega_0$), the capacitor impedance is lower and the voltage lags the current, with the voltage phase angle θ approaching $-90°$.

9-4 LOAD-RESONANT CONVERTERS

In these resonant converters, an *LC* tank is used that results in oscillating load voltage and current and thus provides zero-voltage and/or zero-current switchings. Each circuit in this category is analyzed with a load that is most practical for the converter topology being considered. Only the steady-state operation is considered.

9-4-1 SERIES-LOADED RESONANT dc–dc CONVERTERS

A half-bridge configuration of the SLR converter is shown in Fig. 9-10*a*. The waveforms and the operating principles are the same for the full-bridge configurations. A transformer can be included to provide the output voltage of a desired magnitude as well as the electrical isolation between the input and the output.

The series-resonant tank is formed by L_r and C_r, and the current through the resonant tank circuit is full-wave rectified at the output, and $|i_L|$ feeds the output stage. Therefore, as the name suggests, the output load appears in series with the resonant tank.

The filter capacitor C_f at the output is usually very large, and therefore the output voltage across the capacitor can be assumed to be a dc voltage without any ripple. The

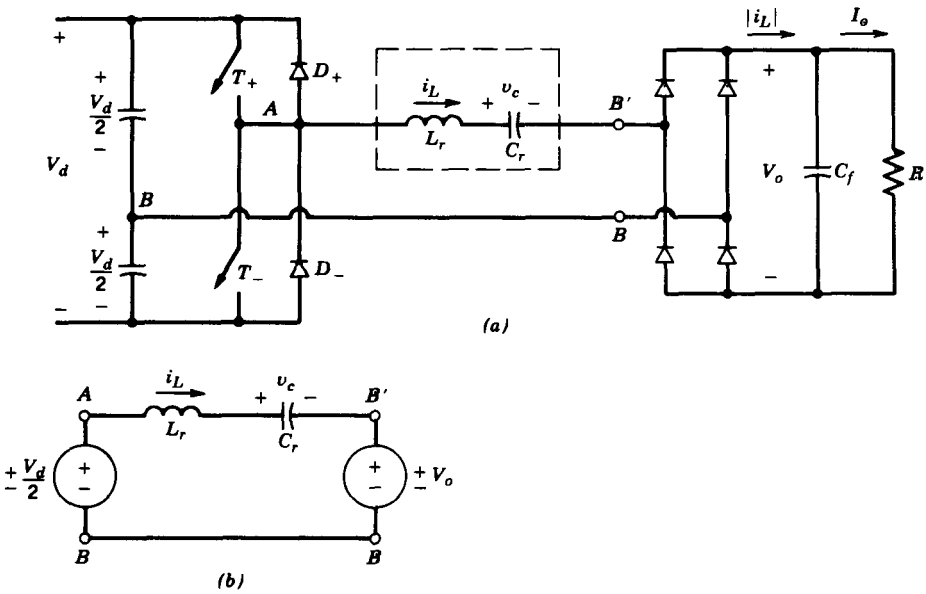


Figure 9-10 SLR dc–dc converter: (*a*) half-bridge; (*b*) equivalent circuit.

resistive power loss in the resonant circuit is assumed to be negligible, which greatly simplifies the analysis. The output voltage V_o is reflected across the rectifier input as $v_{B'B}$, where $v_{B'B} = V_o$ if i_L is positive and $v_{B'B} = -V_o$ if i_L is negative.

When i_L is positive, it flows through T_+ if it is on; otherwise it flows through the diode D_-. Similarly, when i_L is negative, it flows through T_- if it is on; otherwise it flows through the diode D_+. Therefore, in the circuit of Fig. 9-10*a*,

For $i_L > 0$

$$T_+ \text{ conducting:} \quad v_{AB} = +\tfrac{1}{2}V_d \qquad v_{AB'} = +\tfrac{1}{2}V_d - V_o \tag{9-25}$$

$$D_- \text{ conducting:} \quad v_{AB} = -\tfrac{1}{2}V_d \qquad v_{AB'} = -\tfrac{1}{2}V_d - V_o \tag{9-26}$$

For $i_L < 0$

$$T_- \text{ conducting:} \quad v_{AB} = -\tfrac{1}{2}V_d \qquad v_{AB'} = -\tfrac{1}{2}V_d + V_o \tag{9-27}$$

$$D_+ \text{ conducting:} \quad v_{AB} = +\tfrac{1}{2}V_d \qquad v_{AB'} = +\tfrac{1}{2}V_d + V_o \tag{9-28}$$

The foregoing equations show that the voltage applied across the tank ($v_{AB'}$) depends on which device is conducting and on the direction of i_L. The conditions described by Eqs. 7-25 through 9-28 can be represented by an equivalent circuit of Fig. 9-10*b*. The solution for the circuit of Fig. 9-5*a* is applied to the equivalent circuit of Fig. 9-10*b* for each interval, based on the initial conditions and the voltages V_{AB} and $V_{B'B}$, which appear as dc voltages for a given interval.

In the steady-state symmetrical operation, both the switches are operated identically. Similarly, the two diodes operate identically. Therefore, it is sufficient to analyze only one half-cycle of operation, since the other half is symmetrical. It can be shown that in the SLR converter of Fig. 9-10*a*, the output voltage V_o cannot exceed the input voltage $\frac{1}{2}V_d$, that is, $V_o \leq \frac{1}{2}V_d$.

The switching frequency f_s ($=\omega_s/2\pi$), with which the circuit waveforms repeat, can be controlled to be less than or greater than the resonance frequency f_0 ($=\omega_0/2\pi$) if the

converter consists of self-controlled switches. There are three possible modes of operation based on the ratio of switching frequency ω_s to the resonance frequency ω_0, which determines if i_L flows continuously or discontinuously.

9-4-1-1 Discontinuous-Conduction Mode with $\omega_s < \frac{1}{2}\omega_0$

By using Eqs. 9-3 and 9-4, Fig. 9-11 shows the circuit waveforms in steady state where, at $\omega_0 t_0$, switch T_+ is turned on and the inductor current builds up from its zero value. The capacitor voltage builds up from its initial negative value $V_{c0} = -2V_o$. Figure 9-11 also shows the circuits during various intervals with corresponding v_{AB} and $v_{B'B}$.

At $\omega_0 t_1$, 180° subsequent to $\omega_0 t_0$, the inductor current reverses and now must flow through D_+ since the other switch T_- is not yet turned on. After another 180° subsequent to $\omega_0 t_1$ with a smaller peak current in this half-cycle, the current goes to zero and remains zero as no switches are on. A symmetrical operation requires that v_c during the discontinuous interval $\omega_0(t_3-t_2)$ be negative of V_{c0}, that is, equal to $2V_o$. During this interval, the capacitor voltage equal to $2V_o$ is less than $\frac{1}{2}V_d + V_o$ (since $V_o \leq \frac{1}{2}V_d$); therefore the current becomes discontinuous. At $\omega_0 t_3$, the next switch T_- is turned on and the next half-cycle ensues.

Because of the discontinuous interval in Fig. 9-11, one half-cycle of the operating frequency exceeds 360° of the resonance frequency f_0, and therefore in this mode of operation, $\omega_s < \frac{1}{2}\omega_0$. The average of the rectified inductor current $|i_L|$ equals the output dc current I_o, which is supplied to the load at a voltage of V_o.

Note that in this mode of operation, the switches turn off naturally at zero current and at zero voltage, since the inductor current goes through zero. The switches turn on at zero current but not at zero voltage. Also the diodes turn on at zero current and turn off naturally at zero current. Since the switches turn off naturally in this mode of operation, it is possible to use thyristors in low-switching-frequency applications.

The disadvantage of this mode is the relatively large peak current in the circuit and, therefore, higher conduction losses, compared with the continuous-conduction mode.

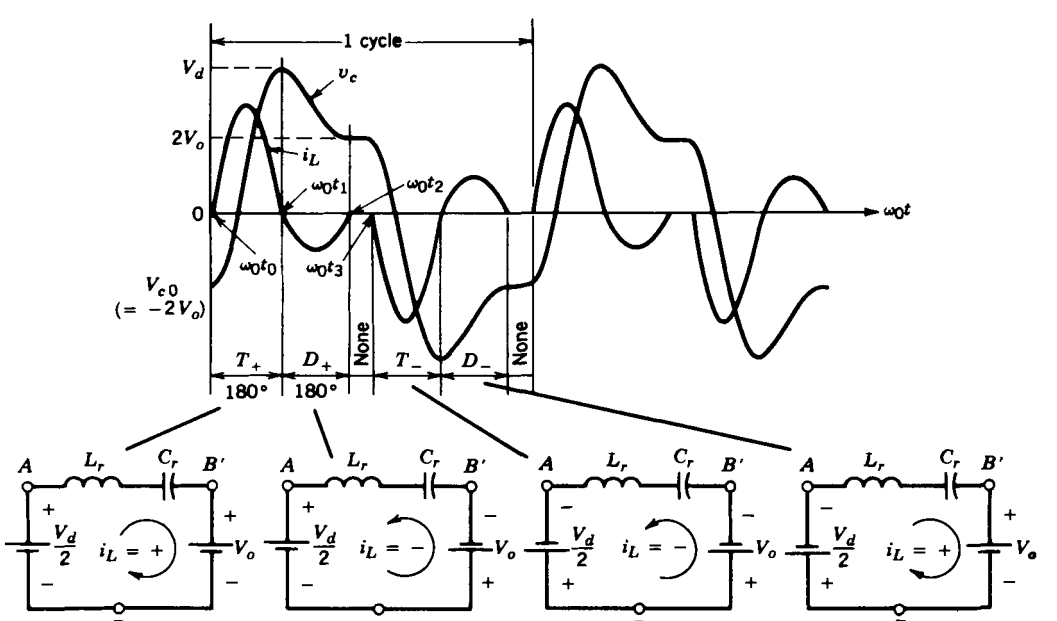


Figure 9-11 SLR dc–dc converter; discontinuous-conduction mode with $\omega_s < \frac{1}{2}\omega_0$.

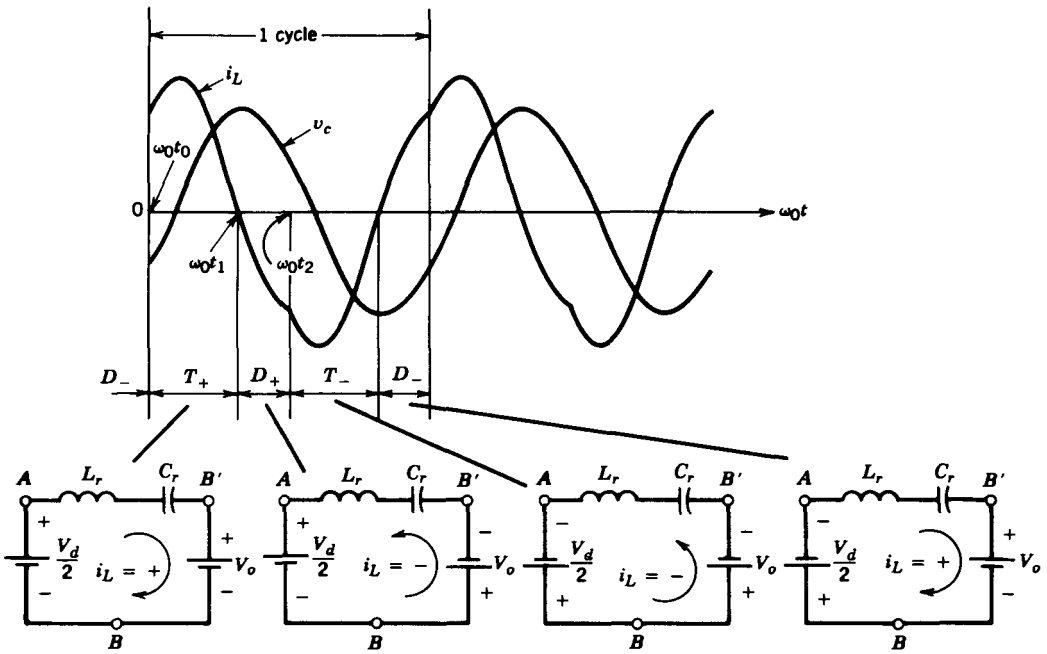


Figure 9-12 SLR dc–dc converter; continuous-conduction mode with $\frac{1}{2}\omega_0 < \omega_s < \omega_0$.

9-4-1-2 Continuous-Conduction Mode with $\frac{1}{2}\omega_0 < \omega_s < \omega_0$

The waveforms are shown in Fig. 9-12 where T_+ turns on at $\omega_0 t_0$, with a finite value of the inductor current and at a preconduction switch voltage of V_d. Here T_+ conducts for less than 180°. At $\omega_0 t_1$, i_L reverses and flows through D_+, thus naturally turning off T_+. At $\omega_0 t_2$, T_- is turned on and i_L transfers from D_+ to T_-. In this mode, D_+ conducts for less than 180° because T_- is switched on early, compared with the discontinuous-conduction mode.

In this mode of operation, the switches turn on at a finite current and at a finite voltage, thus resulting in a turn-on switching loss. Moreover, the freewheeling diodes must have good reverse-recovery characteristics to avoid large reverse current spikes flowing through the switches, for example, at $\omega_0 t_2$ through D_+ and T_-, and to minimize the diode turn-off losses. However, the turn-off switches occurs naturally at zero current and at zero voltage as the inductor current through them goes to zero and reverses through the freewheeling diodes. Therefore, it is possible to use thyristors as switches in low-switching-frequency applications.

9-4-1-3 Continuous-Conduction Mode with $\omega_s > \omega_0$

Compared with the previous continous-conduction mode, where the switches turn off naturally but turn on at a finite current, the switches in this mode with $\omega_s > \omega_0$ are forced to turn off a finite current, but they are turned on at zero current and zero voltage.

Figure 9-13 shows the circuit waveforms where T_+ starts conduction at $\omega_0 t_0$ at zero current when the inductor current reverses in direction. At $\omega_0 t_0$, before the half-cycle of the current oscillation ends, T_+ is forced to turn off, thus forcing the positive i_L to flow through D_-. Because of the large negative dc voltage applied across the LC tank ($v_{AB'} = -\frac{1}{2}V_d - V_o$), the current through the diode goes to zero quickly (note that its frequency

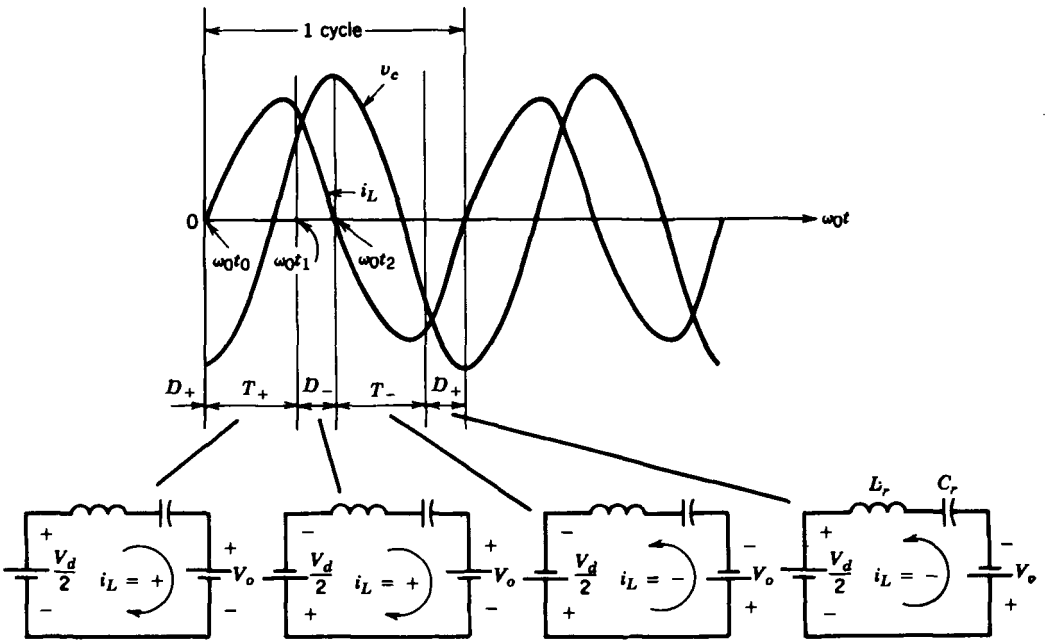


Figure 9-13 SLR dc–dc converter; continuous-conduction mode with $\omega_s > \omega_0$.

of oscillation ω_0 does not change) at $\omega_0 t_2$. Here T_- is gated on as soon as D_- begins to conduct so that it can conduct when i_L reverses. The combined conduction interval for T_+ and D_- is equal to one half-cycle of operation at the switching frequency of ω_s. This half-cycle is less than 180° of the resonance frequency ω_0, thus resulting in $\omega_s > \omega_0$.

There are several advantages in operating at $\omega_s > \omega_0$. Unlike the continuous-conduction mode with ω_s less than ω_0, the switches turn on at a zero current and zero voltage; thus, the freewheeling diodes do not need to have very fast reverse-recovery characteristics. A significant disadvantage would appear to be that the switches need to force turn off near the peak of i_L, thus causing a large turn-off switching loss. However, since the switches turn on not only at zero current but also at zero voltage (note that prior to turn-on of T_-, the freewheeling diode D_- across it is conducting), it is possible to use lossless snubber capacitors C_s in parallel with the switches, as shown in Fig. 9-14, which act as lossless turn-off snubbers for the switches.

Operation above the resonance frequency requires that the controllable switches be used.

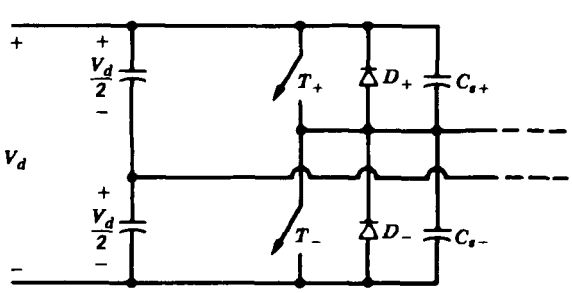


Figure 9-14 Lossless snubbers in an SLR converter at $\omega_s > \omega_0$.

9-4-1-4 Steady-State Operating Characteristics

It is useful to know the relationship of the peak and the average values of the circuit voltages and currents to the operating conditions (V_d, V_o, I_o, ω_0, etc.). The voltages, currents, and switching angular frequency ω_s are normalized by the following base quantities:

$$V_{\text{base}} = \tfrac{1}{2}V_d \tag{9-29}$$

$$I_{\text{base}} = \frac{\tfrac{1}{2}V_d}{Z_0} \tag{9-30}$$

$$\omega_{\text{base}} = \omega_0 \tag{9-31}$$

Figure 9-15 shows normalized I_o versus ω_0 for two values of V_o. This figure shows that a SLR dc–dc converter in the discontinuous-conduction mode (corresponding to $\omega_s < 0.5$) operates as a current source, that is, I_o stays constant even though the load resistance and hence V_o may change. Because of this property, this converter exhibits an inherent overload protection capability in the discontinuous-conduction mode.

It should be noted that in Fig. 9-10*a*, I_o is the average value of the full-wave-rectified inductor current $|i_L|$, where the ripple in $|i_L|$ is assumed to flow through the output filter capacitor and its average value I_o flows through the output load resistance. In this converter, the peak value of the inductor current (which also is the peak value of the current through the switches) and the peak voltage across the capacitor C_r can be several times higher than I_o and V_d, respectively (see the problems at the end of the chapter). This aspect must be considered in comparing this converter with other converter topologies.

9-4-1-5 Control of SLR dc–dc Converters

As shown in Section 9-3-1-3 dealing with the frequency characteristics of series-resonant circuits, the resonant-tank impedance depends on the frequency of operation. Therefore, for a given applied input voltage V_d and a load resistance, V_o can be regulated by controlling the switching frequency f_s. This is shown in block diagram form in Fig. 9-16,

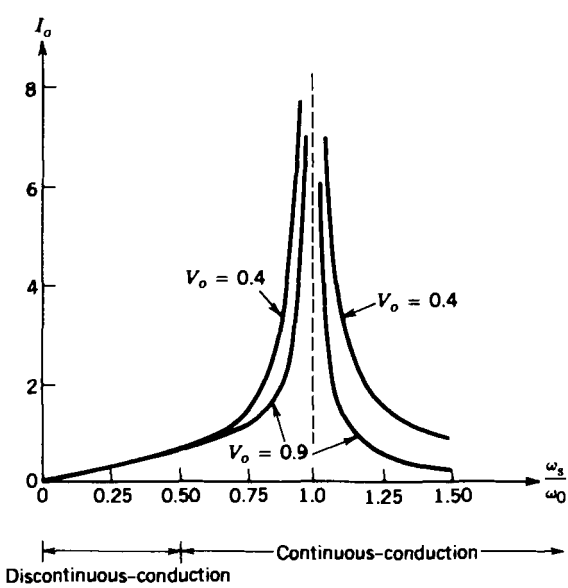


Figure 9-15 Steady-state characteristics of an SLR dc–dc converter; all parameters are normalized.

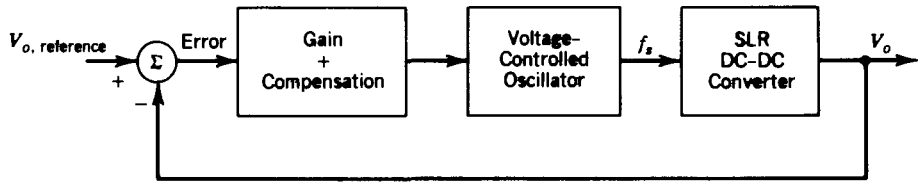


Figure 9-16 Control of SLR dc–dc converter.

where the error between the sensed output voltage and the reference voltage determines the output frequency f_s of the voltage-controlled oscillator, which in turn controls the two switches.

The variable frequency control described before is not optimum because of the complexity of its analysis and the design of EMI filters. As discussed in reference 7, a constant frequency control can be implemented in a full-bridge version of the SLR converter, where the switches in each leg of the converter operate at the 50% duty ratio at a constant frequency of $\omega_s > \omega_0$, but the phase delay between the output of the two converter legs is controlled. Such a control restricts the load to be in a limited range, beyond which the zero-voltage-/zero-current-switching characteristics of the converter do not hold.

It should be noted that the SLR converter can be used where the output is not a rectified dc; for example, SLR inverters are used for induction heating applications, where the load appears as a resistance rather than a dc voltage V_o.

9-4-2 PARALLEL-LOADED RESONANT dc–dc CONVERTERS

These converters are similar to the SLR converters in terms of operating with a series-resonant *LC* tank circuit. However, unlike the SLR converters, where the output stage or the load appears in series with the resonant tank, here the output stage is connected in parallel with the resonant-tank capacitor C_r, as shown in Fig. 9-17*a*. The isolation transformer is omitted for simplicity.

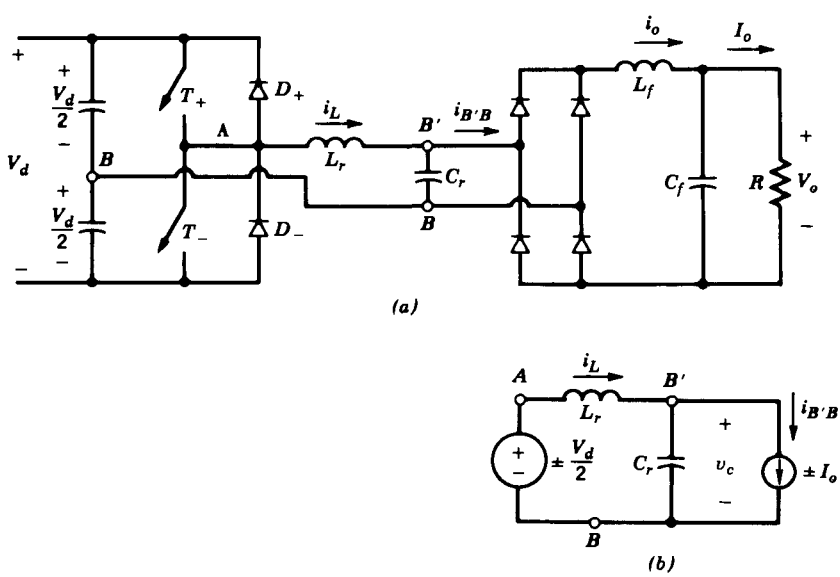


Figure 9-17 PLR dc–dc converter: (*a*) half-bridge; (*b*) equivalent circuit.

The PLR converters differ from the SLR converters in many important respects, for example, (1) PLR converters appear as a voltage source and hence, are better suited for multiple outlets; (2) unlike the SLR converters, the PLR converters do not possess inherent short-circuit protection capability, which obviously is a drawback; and (3) PLR converters can step up as well as step down the voltage, unlike the SLR converters, which can operate only as a step-down converter (not counting the transformer turns ratio).

In the following sections, only the modes in which a PLR converter is likely to operate are discussed. The discussion on the other modes can be found in the literature.

The voltage across the resonant-tank capacitor C_r is rectified, filtered, and then supplied to the load. To develop an equivalent circuit, the current through the output filter inductor in Fig. 9-17*a* can be assumed to be a ripple-free dc current I_o during a switching-frequency time period. This is a reasonable assumption, based on a high switching frequency and a sufficiently large value of the filter inductor. The voltage across the resonant tank depends on the devices conducting as follows:

$$T_+ \text{ or } D_+: \qquad v_{AB} = +\tfrac{1}{2}V_d \tag{9-32}$$

and

$$T_- \text{ or } D_-: \qquad v_{AB} = -\tfrac{1}{2}V_d \tag{9-33}$$

Based on the previous discussion, an equivalent circuit of Fig. 9-17*b* can be obtained where the input voltage to the tank (v_{AB}) is equal in magnitude to $\frac{1}{2}V_d$ but its polarity depends on which switch is turned on (T_+ or T_-). The current $i_{B'B}$, defined in Fig. 9-17*a*, equals I_o in magnitude, but its direction depends on the polarity of the voltage v_c across C_r at the input to the bridge rectifier.

The equivalent circuit of Fig. 9-17*b* is identical to that discussed in Section 9-3-1-2. Therefore, Eqs. 9-13 and 9-14 can be applied with the appropriate v_{AB} and $i_{B'B}$ and the initial conditions.

Unlike SLR converters, a PLR dc–dc converter can operate in a large number of combinations consisting of the states of i_L and v_c. However, only three modes are considered in the following sections.

9-4-2-1 Discontinuous Mode of Operation

In this mode of operation, both i_L and v_c remain zero simultaneously for some length of time. The steady-state waveforms for this mode of operation are plotted in Fig. 9-18, based on Eqs. 9-13 and 9-14. During steady-state operation, initially both i_L and v_c are zero and T_+ is turned on at $\omega_0 t_0$. So long as $|i_L| < I_o$, the output current circulates through the rectifier bridge, which appears as a short circuit across C_r and keeps its voltage at zero, as shown in Fig. 9-18. At $\omega_0 t_1$, i_L exceeds I_o and the difference $i_L - I_o$ flows through C_r, and v_c increases. Due to LC resonance, i_L reverses at $\omega_0 t_2$ and flows through D_+, since T_- is not turned on until some time later. During the interval $\omega_0(t_3 - t_1)$, i_L and v_c can be calculated from Eqs. 9-13 and 9-14 using $i_{L0} = I_o$ and $v_{c0} = 0$ as the initial conditions at time $\omega_0 t_1$. If the gate/base drive of T_+ is removed prior to $\omega_0 t_3$, i_L can no longer flow after $\omega_0 t_3$ and stays at zero. With $i_L = 0$, i_o flows through C_r, and v_c decays linearly to zero during the interval $\omega_0 t_3$ to $\omega_0 t_4$.

In this discontinuous mode of operation, both v_c and i_L stay at zero for an interval that can be varied in order to control the output voltage. Beyond this discontinuous interval, T_- is gated on at $\omega_0 t_5$ and the next half-cycle ensues with identical initial conditions of zero i_L and v_c as for the first half-cycle.

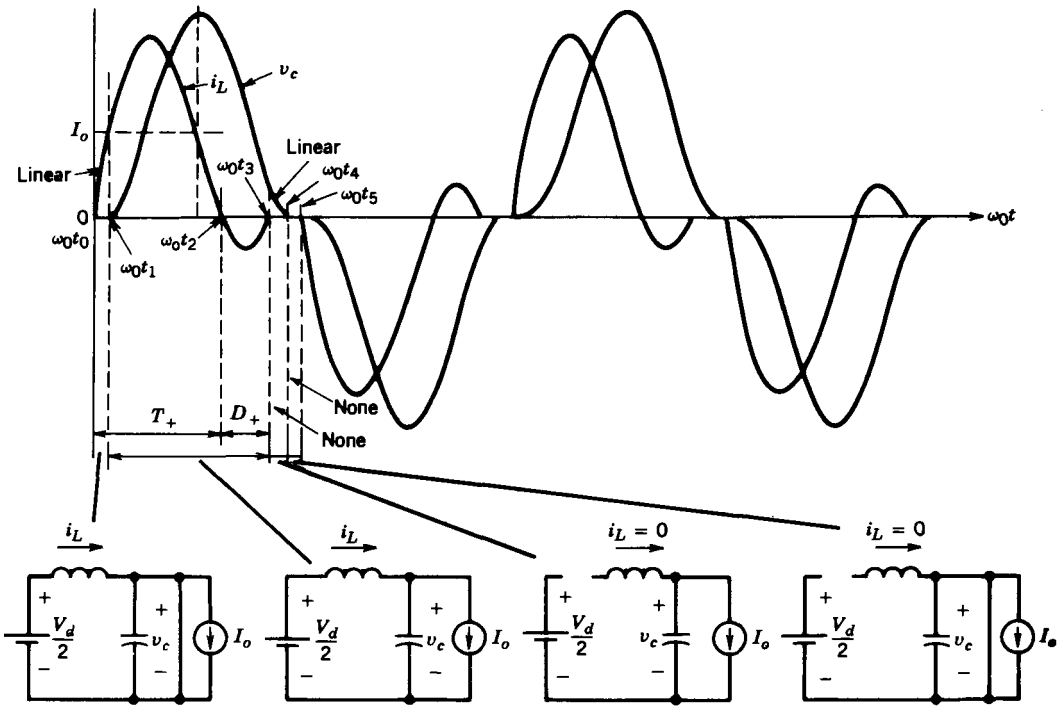


Figure 9-18 PLR dc–dc converter in a discontinuous mode.

Clearly, the foregoing operation corresponds to ω_s in a range from zero to approximately $\frac{1}{2}\omega_0$. Also, there are no turn-on or turn-off stresses on the switches or the diodes.

9-4-2-2 Continuous Mode of Operation Below ω_0

At switching frequencies higher than those in the discontinuous mode but less than ω_0, both v_c and i_L becomes continuous. The waveforms are shown in Fig. 9-19, where a switch turns on at a finite i_L and the current commutates from the diode connected in antiparallel with the other switch. This results in turn-on losses in the switches, and the diodes must have good reverse-recovery characteristics. However, there are no turn-off losses in the switches since the current through them commutates naturally when i_L reverses in direction.

9-4-2-3 Continuous Mode of Operation Above ω_0

This mode with continuous v_c and i_L occurs at $\omega_s > \omega_0$. The circuit waveforms are shown in Fig. 9-20. Here, the turn-on losses in the switches are eliminated since the switches turn on naturally when i_L, initially flowing through the diodes, reverses. However, this operating mode results in the turn-off losses in the switches, since a switch is forced to turn off, thus transferring its current to the diode connected in antiparallel with the other switch.

Similar to the SLR converter operating in a continuous-conduction mode with $\omega_s > \omega_0$, the switches here turn on at zero voltage, thus at the switching instant the snubber capacitor in parallel has no stored energy. Therefore, it is possible to eliminate the turn-off

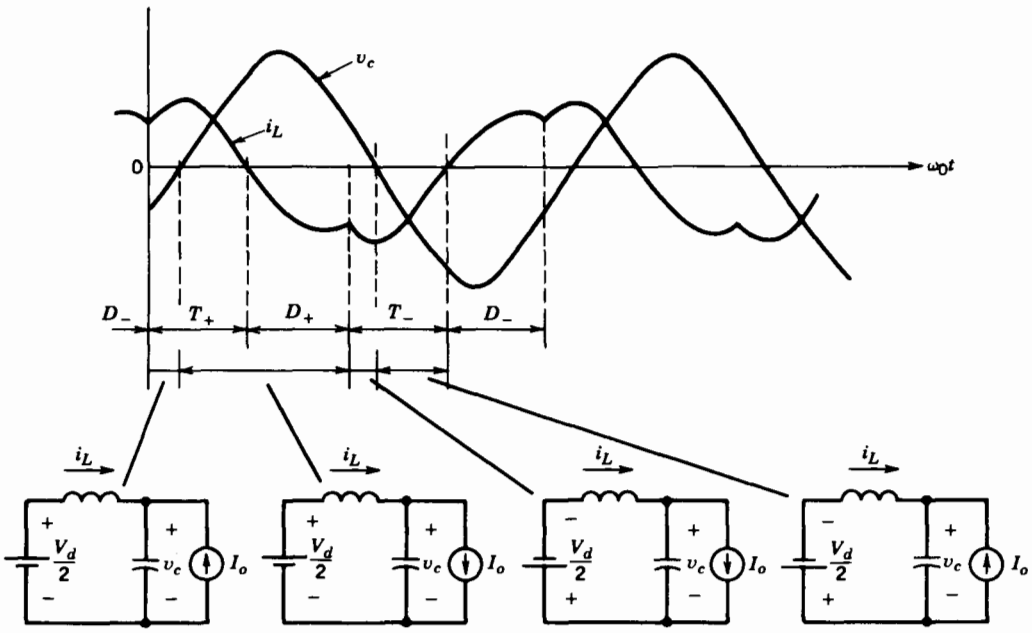


Figure 9-19 PLR dc–dc converter in a continuous mode with $\omega_s < \omega_0$.

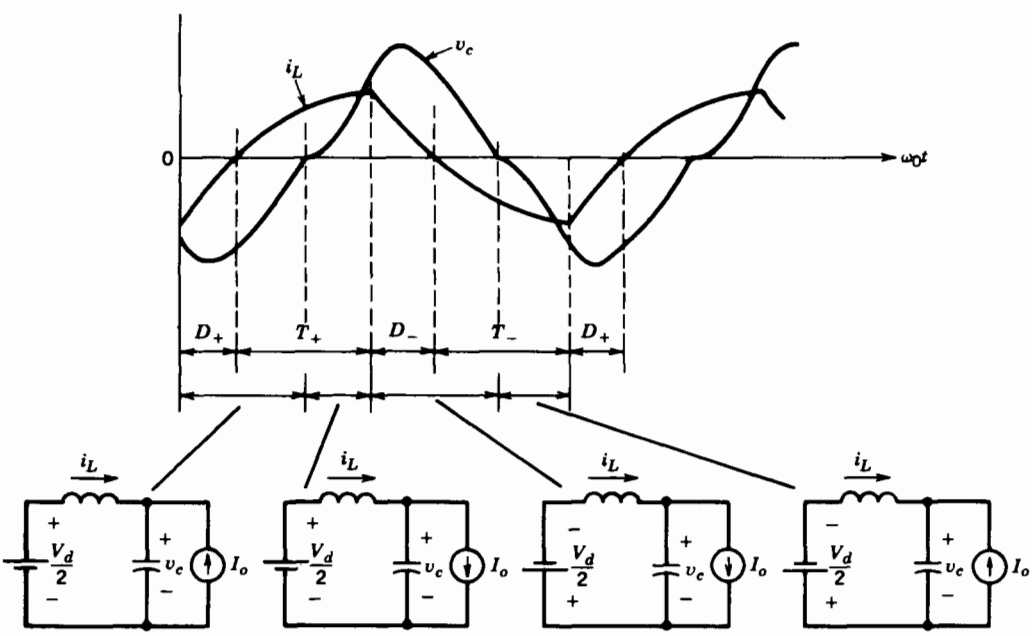


Figure 9-20 PLR dc–dc converter in a continuous mode with $\omega_s > \omega_0$.

losses by connecting a lossless snubber consisting of a capacitor (with no series resistor) in parallel with each switch, as in an SLR converter in Fig. 9-14.

9-4-2-4 Steady-State Operating Characteristics

The steady-state operating characteristics of the PLR dc–dc converters are shown in Fig. 9-21 for two values of I_o, where the variables are normalized by using the base quantities

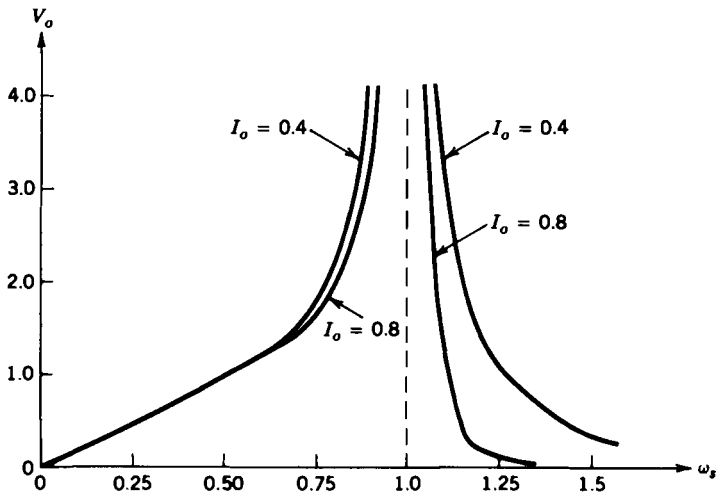


Figure 9-21 Steady-state characteristics of a PLR dc–dc converter. All quantities are normalized.

defined in Eqs. 9-29 through 9-31. Figure 9-21 shows the following important properties of the PLR converter:

- In the discontinuous mode of operation with $\omega_s < \frac{1}{2}\omega_0$, this converter exhibits a good voltage source characteristic and V_o remains independent of I_o. This property is useful in designing a converter with multiple outputs.
- Also in the frequency range $\omega_s < \frac{1}{2}\omega_0$, the output varies linearly with ω_s, thus simplifying the output regulation.
- It is also possible to operate in the high-frequency range $\omega_s > \omega_0$, and the maximum change required in the operating frequency is less than 50% to compensate for the output loading for a normalized output voltage of 1.0.
- It is possible to step up or step down the output voltage, that is, V_o can be less than or greater than 1.0.

In this converter, the peak inductor current (which is also the peak current through the switches) and the peak capacitor voltage can be several times higher than I_o and V_{dc}, respectively (see the problems).

The converter characteristics shown in Fig. 9-21 suggest than an effective way to regulate the output is by controlling the frequency of operation ω_s.

9-4-3 HYBRID-RESONANT dc–dc CONVERTER

This topology consists of a series-resonant circuit as shown in Fig. 9-22 but the load is connected in parallel with only part of the capacitance, for example, one-third of the total capacitance, and the other two-thirds of the capacitance appears in series. The purpose of this topology is to benefit from the advantageous properties of both the SLR and the PLR converters, namely that an SLR converter offers an inherent current limiting under short-circuit conditions and a PLR converter acts as a voltage source, and thus regulating its voltage at no load with a high-Q resonant tank is not a problem. These converters can be analyzed based on the discussion presented in the previous two sections. These are analyzed in detail in reference 15.

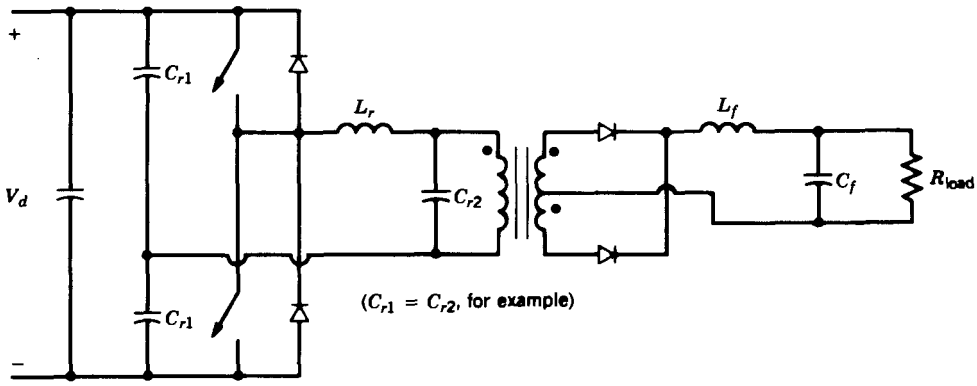


Figure 9-22 Hybrid-resonant dc–dc converter.

9-4-4 CURRENT-SOURCE, PARALLEL-RESONANT dc-TO-ac INVERTERS FOR INDUCTION HEATING

The basic principle of such an inverter is illustrated by means of the circuit of Fig. 9-23*a*, where a square-wave current source is applied to a parallel-resonant load. The induction coil and the load (*RL* combination) are modeled by means of a parallel combination of equivalent R_{load} and L_r, rather than a series *RL*. The capacitor C_r is added to resonate with L_r, rather than a series *RL*. The capacitor C_r is added to resonate with L_r in parallel. It is assumed that the harmonic impedance of the parallel-resonant load at the harmonic frequencies of the input current source is negligibly small, thus resulting in an essentially sinusoidal voltage v_o. Therefore, the analysis of Section 9-3-2-2 applies.

When the fundamental frequency ω_s of the source current i_o equals the natural resonance frequency $\omega_0 = (1/\sqrt{L_rC_r})$, the circuit phasor diagram is shown in Fig. 9-23*b*, where the fundamental-frequency component $\mathbf{V}_{o1}$ of the resulting voltage is in phase with the fundamental-frequency component $\mathbf{I}_{o1}$ of the input current.

Since the square-wave input current in practice is supplied by a thyristor inverter, the resonant load must supply the capacitive vars to the inverter. This implies that the load voltage $\mathbf{V}_{o1}$ should lag the input current $\mathbf{I}_{o1}$, which is possible only at a frequency $\omega_s > \omega_0$, as shown in Fig. 9-23*c*.

A current-source inverter consisting of thyristors is shown in Fig. 9-24*a*. To avoid a large *di/dt* (during current commutation) through the inverter thyristors, a small inductance L_c in series with the resonant load is purposely introduced. The inverter output

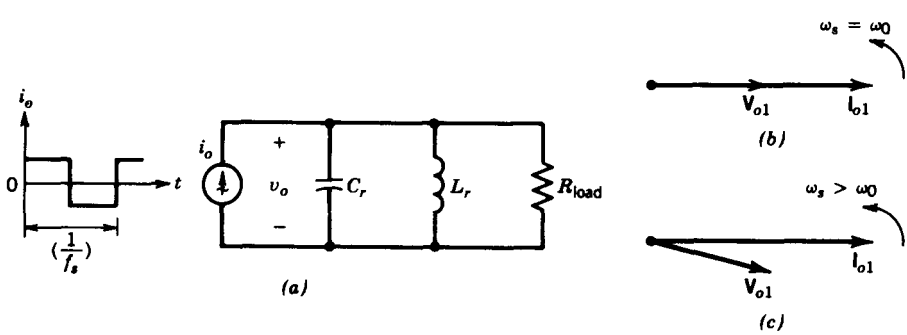


Figure 9-23 Basic circuit for current-source, parallel-resonant converter for induction heating: (*a*) basic circuit; (*b*) phasor diagram at $\omega_s = \omega_0$; (*c*) phasor diagram at $\omega_s > \omega_0$.

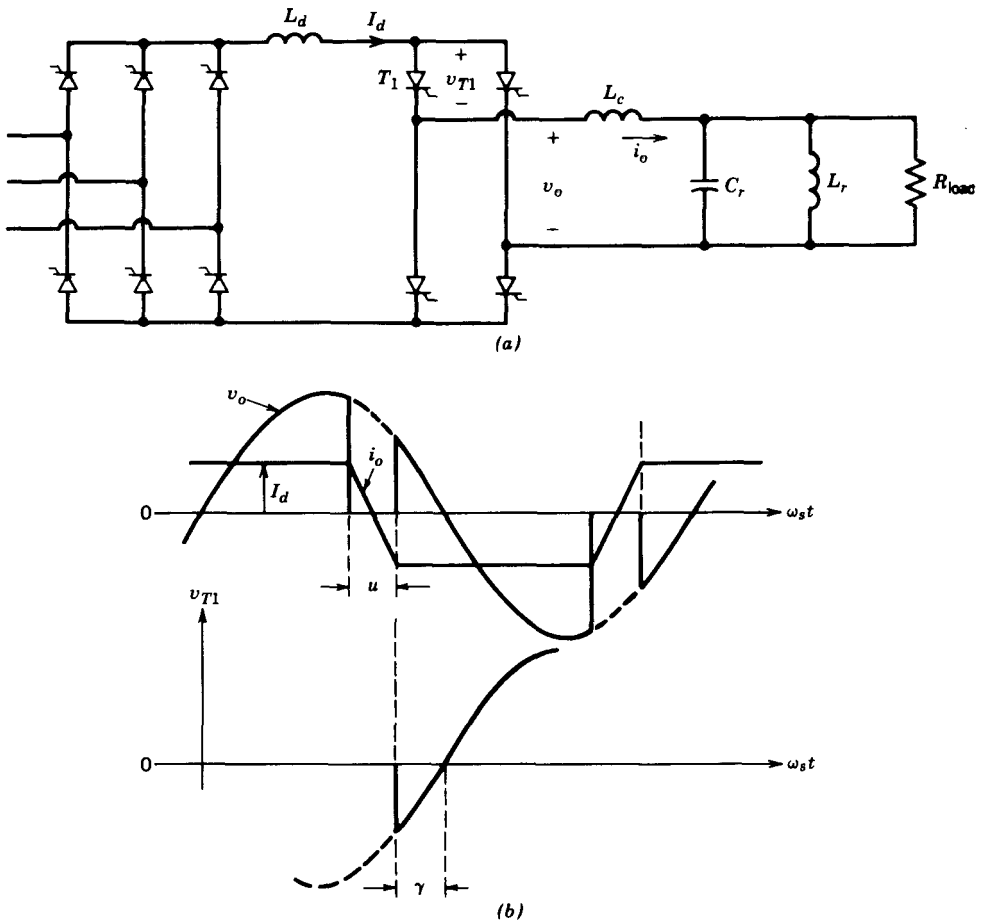


Figure 9-24 Current-source, parallel-resonant inverter for induction heating: (*a*) circuit; (*b*) waveforms.

current i_o therefore deviates from its idealized square-wave shape and becomes trapezoidal, as shown in Fig. 9-24*b*.

The voltage across one of the thyristors T_1 shows that after it stops conducting a reverse voltage appears across it for a time interval equal to γ/ω_s; subsequently it is required to block a forward-polarity voltage. Therefore, γ/ω_s should be sufficiently larger than the specified turn-off time t_q of the thyristor that is being used.

One of the techniques to control the power output of this inverter is by controlling its switching frequency. As the switching frequency f_s is increased further above the natural resonance frequency f_0, the power output decreases if I_d is held constant by means of a controlled dc supply. Another obvious technique to control the power output is to control I_d, keeping the switching frequency of the inverter constant.

9-4-4-1 Start-up

In case of a current-fed parallel-resonant inverter, the load must be in resonance with C_r prior to the inverter operation in Fig. 9-24*a*. This is accomplished by means of a precharged capacitor dumping its charge onto the parallel-resonant load circuit, thus establishing oscillating load voltages and currents. Shortly after that, the inverter operation is initiated.

9-4-5 CLASS E CONVERTERS

In class E converters, the load is supplied through the sharply tuned series-resonant circuit shown in Fig. 9-25*a*. This results in an essentially sinusoidal current i_o. The input to the converter is through a sufficiently large inductor to allow the assumption that in steady state, the input to the converter is a dc current source I_d, as shown in Fig. 9-25*a*, where the current magnitude depends on the power output. The waveforms are shown in Fig. 9-25*b* for an optimum mode, which is discussed later on. When the switch is on, $I_d + i_o$ flows through the switch, as shown in Fig. 9-25*c*. When the switch is turned off, because of the capacitor C_1, the voltage across the switch builds up slowly, thus allowing a zero-voltage turn-off of the switch. With the switch off, the oscillating circuit is as shown in Fig. 9-25*d*, where the voltage across capacitor C_1 builds up, reaches its peak, and eventually comes back to zero, at which instant the switch is turned back on.

A class E converter operates at a switching f_s, which is slightly higher than the resonant frequency $f_0 = 1/(2\pi\sqrt{L_r C_r})$. During the interval when the switch is off, the

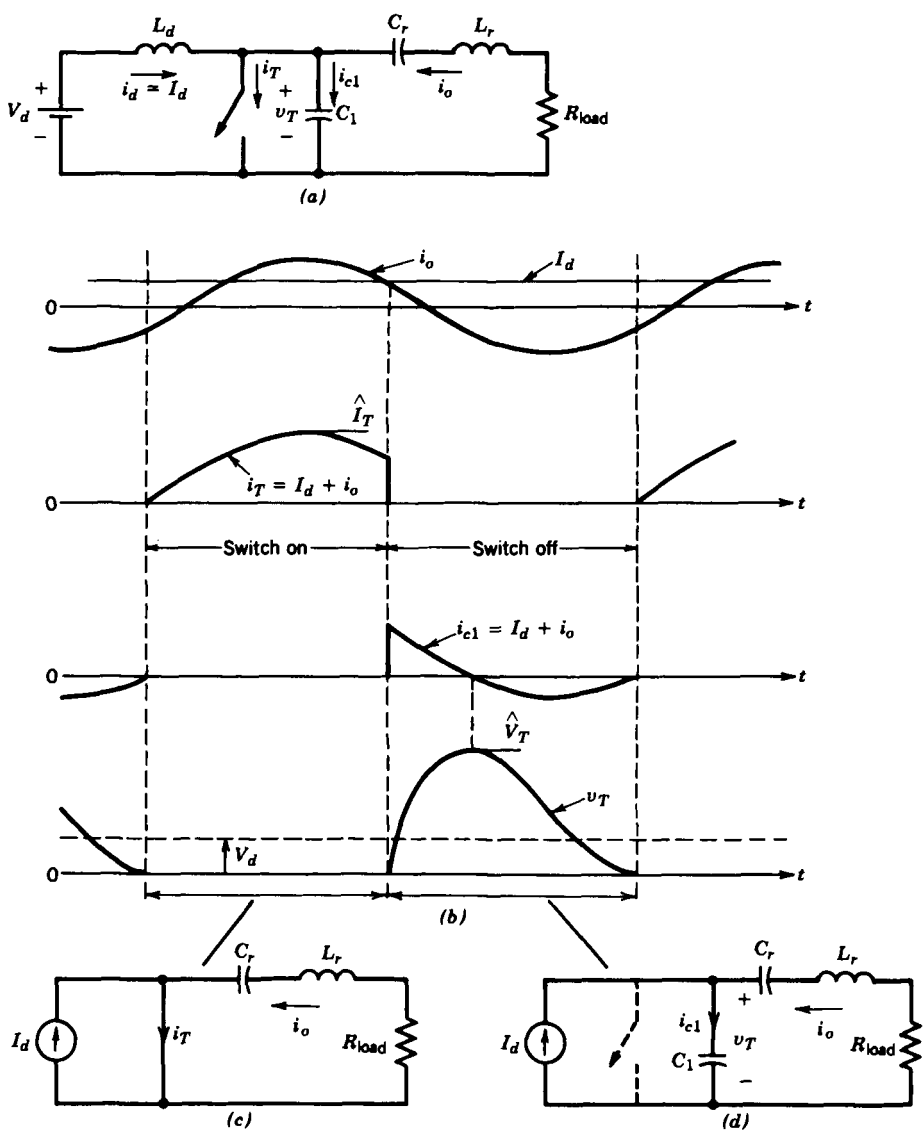


Figure 9-25 Class E converter (optimum mode, $D = 0.5$).

input supplies power to the circuit since v_T is positive, as shown in Fig. 9-25*b*. For a high-quality factor of the series L_rC_rR circuit ($Q \geq 7$), which results in an essentially sinusoidal load current i_o, only a slight variation in f_s is needed to vary the output voltage. As f_s increases (where $f_s > f_0$), i_o and therefore v_R decrease.

Another observation that can be made is as follows: The average value of v_T equals V_d. If i_o is assumed to be purely sinusoidal, the average voltage across the load resistance R is zero. The average voltage across L_r is also zero in steady state. Therefore, C_r blocks the dc voltage V_d in addition to providing a resonant circuit.

The operation of a class E converter can be categorized in optimum and suboptimum modes. The circuit and the waveforms shown in Fig. 9-25 belong to the optimum mode of operation where the switch voltage returns to zero with a zero slope ($i_{c1} = 0$) and there is no need for a diode in antiparallel with the switch. This mode of operation requires that the load resistance R be equal to an optimum value R_{opt}. The switch duty ratio $D = 0.5$ results in a maximum power capability or, in other words, the maximum switch utilization ratio, where the switch utilization ratio is defined as the ratio of the output power P_o to the product of the peak switch voltage and the peak switch current. It is shown in the literature that the peak switch current is approximately $3I_d$ and the peak switch voltage is approximately $3.5V_d$.

The nonoptimum mode of operation occurs if $R < R_{opt}$. Here, the switch voltage reaches zero with a negative slope [$dv_T/dt < 0$, and hence, $i_{c1} = C_1(dv_T/dt) < 0$]. A diode is connected in antiparallel with the switch as shown in Fig. 9-26*a* to allow this

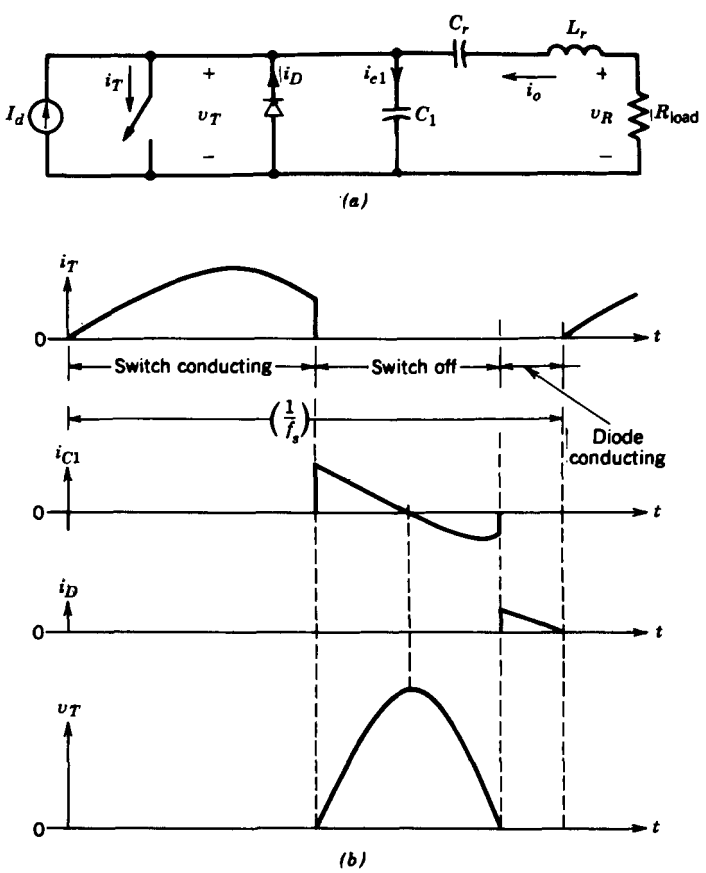


Figure 9-26 Class E converter (nonoptimum mode).

current to flow while keeping the switch voltage at zero (at one diode drop). The waveforms are shown in Fig. 9-26*b*, where the switch is turned on as soon as the diode starts to conduct. In a circuit with a high input voltage, it is important to reduce the peak switch voltage $\hat{V}_T$. It can be shown that for a smaller switch duty ratio, $\hat{V}_T$ decreases but the peak switch current $\hat{I}_T$ goes up.

The advantage of a class E converter is the elimination of switching losses and the reduction in EMI. Also, it is a single-switch topology and produces a sinusoidal output current. Significant disadvantages are high peak voltage and current associated with the switch and large voltages and currents through the resonant *LC* elements. For the resistive load shown in Fig. 9-26*a* (the optimum mode without an antiparallel diode with the switch is very restrictive), class E converters have been considered for high-frequency electronic lamp ballasts.

It is possible to obtain a dc–dc voltage conversion by rectifying the output current. Since the output load may vary over a large range, an impedance matching network is required between the output of the class E converter and the output rectification stage to ensure a lossless switching operation of the class E converter. Various suboptimum class E topologies are described in reference 22.

9-5 RESONANT-SWITCH CONVERTERS

Historically, prior to the availability of controllable switches with appreciable voltage- and current-handling capability, the switch-mode converters consisted of thyristors (currently, thyristors in switch-mode converters are used only at very high power levels). Such converters had topologies and control schemes similar to those described in Chapters 7 and 8 for switch-mode dc–dc converters and dc-to-ac inverters. Each thyristor in such a converter required a current commutation circuit, which consisted of an *LC* resonant circuit plus other auxillary thyristors and diodes, which turned the main thyristor off by forcing the current through it to go to zero. Because of the complexity and substantial losses in the commutation circuits, thyristors were replaced by controllable switches, as their power-handling capability improved.

A need to increase switching frequencies and to reduce EMI led to augmenting the controllable switches in certain basic switch-mode converter topologies of Chapters 7 and 8 by a simple *LC* resonant circuit, thereby shaping the switch voltage and current in order to yield zero-voltage and/or zero-current switchings. Such converters are termed resonant-switch converters. Often, the diode needed for the resonant-switch circuit operation is the same as that in the original switch-mode converter topology. Similarly, inductors (such as the transformer leakage inductance) and the capacitors (such as the output capacitance of the semiconductor switch), which appear as undesirable parasitics in switch-mode topologies, can be utilized to provide the resonant inductor and the capacitor needed for the resonant-switch circuit.

The output in some of these circuits is controlled by controlling the operating frequency; in others a constant-frequency square-wave or PWM control can be used with some additional constraints to provide zero-voltage and/or zero-current switchings.

A majority of such converters can be divided into three switching categories:

1. Zero-current-switching (ZCS) topology where the switch turns on and turns off at zero current. The peak resonant current flows through the switch but the peak switch voltage remains the same as in its switch-mode counterpart. Such a topology is shown in Fig. 9-27*a* for a step-down dc–dc converter.
2. Zero-voltage-switching (ZVS) topology where the switch turns on and turns off at zero voltage. The peak resonant voltage appears across the switch, but the peak

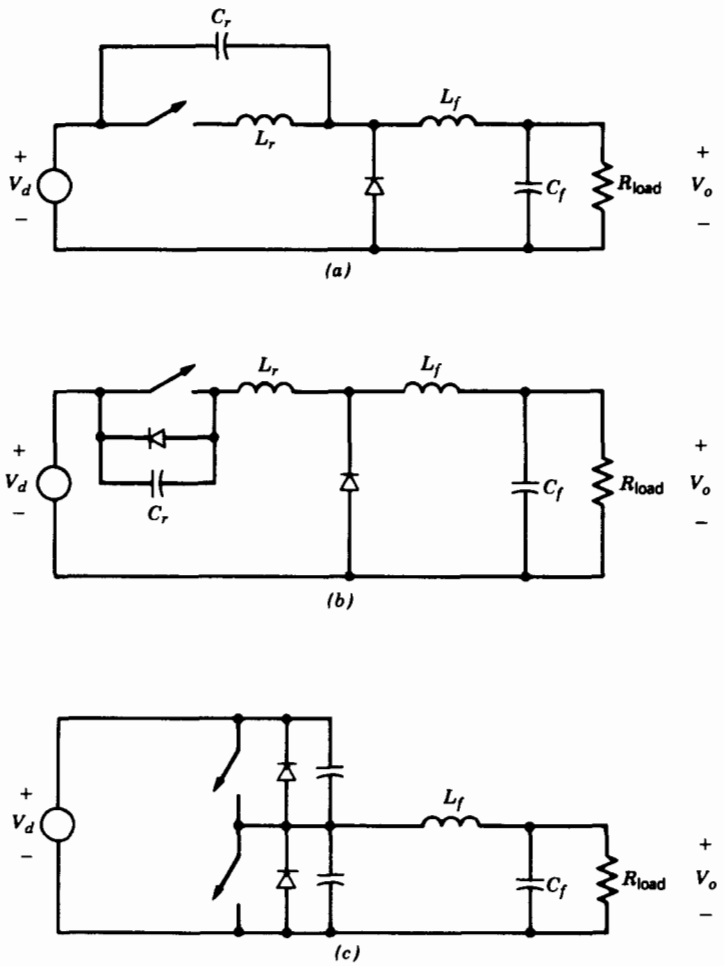


Figure 9-27 Resonant-switch converters: (a) ZCS dc–dc converter (step-down); (*b*) ZVS dc–dc converter (step-down); (*c*) ZVS-CV dc–dc converter (step-down).

switch current remains the same as in its switch-mode counterpart. Such a topology is shown in Fig. 9-27*b* for a step-down dc–dc converter.

3. Zero-voltage-switching, clamped-voltage (ZVS-CV) topology where the switch turns on and off at zero voltage as in category 2 above. However, a converter of this topology consists of at least one converter leg made up of two such switches. The peak switch voltage remains the same as in its switch-mode counterpart, but the peak switch current is generally higher. Such a converter topology is shown in Fig. 9-27*c* for a step-down dc–dc converter.

In the following sections, the operating principles of the converters belonging to all three switching categories are discussed.

9-5-1 ZCS RESONANT-SWITCH CONVERTERS

In such converters, the current produced by *LC* resonance flows through the switch, thus causing it to turn on and off at zero current. This can be easily explained in the step-down dc–dc converter of Fig. 9-28*a*, which has been modified as shown in Fig. 9-28*b* by the

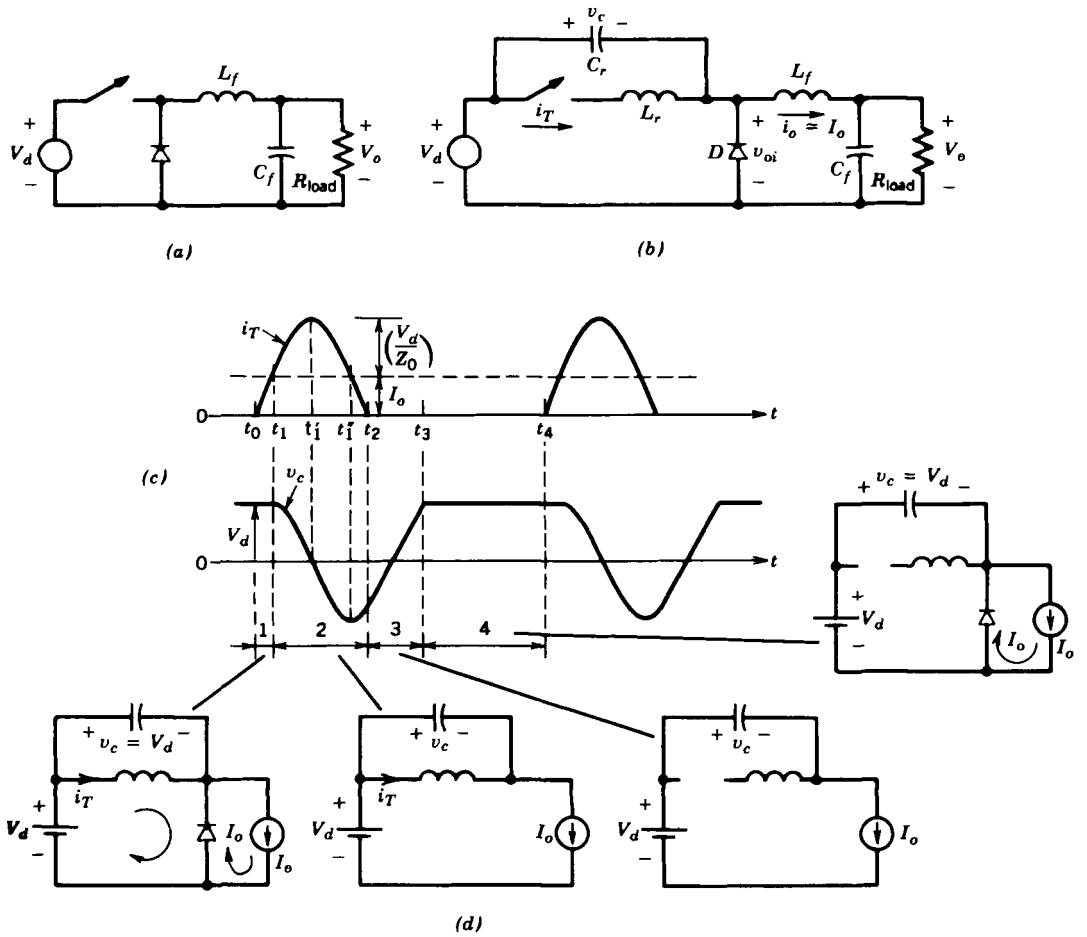


Figure 9-28 ZCS resonant-switch dc–dc converter.

addition of L_r and C_r. The filter inductor L_f is sufficiently large such that the current i_o can be assumed to be a current of constant magnitude I_o in Fig. 9-28*b*. The circuit waveforms in steady state are shown in Fig. 9-28*c* and the subcircuits are shown in Fig. 9-28*d*.

Prior to turning the switch on, the output current I_o freewheels through the diode D, and the voltage v_c across C_r equals V_d. At t_0, the switch is turned on at zero current. So long as i_T is less than I_o, D keeps on conducting and v_c stays at V_d. Therefore, i_T rises linearly, and at t_1, i_T equals I_o, which causes D to stop conducting. Now, L_r and C_r form a parallel-resonant circuit and the analysis of Section 9-3-2-1 applies. Use of Eq. 9-20 shows that at t_1', i_T peaks at $V_d/Z_0 + I_o$ and v_c reaches zero. The negative peak of v_c occurs at t_1'' when $i_T = I_o$. At t_2, i_T reaches zero and cannot reverse its direction. Thus the switch T is naturally turned off. Beyond t_2, the gate pulse from T is removed. Now I_o flows through C_r and v_c rises linearly to V_d at t_3, at which point the diode D turns on and v_c stays at V_d. After an interval during which i_T is zero and $v_c = V_d$, the gate pulse to T is again applied at t_4 to turn it on, and the next cycle ensues.

It is clear from the waveforms of Fig. 9-28*c* that the forward switch voltage is limited to V_d. The instantaneous voltage $v_{oi} = V_d - v_c$ across the output diode, as defined as Fig. 9-28*b*, is plotted in Fig. 9-29. By controlling the switch-off time interval $t_4 - t_3$, or in other words the switching frequency of operation, the average value of v_{oi} and, hence, the

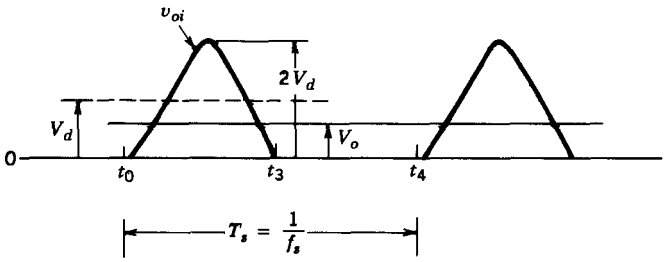


Figure 9-29 v_{oi} waveform in a ZCS resonant-switch dc–dc converter.

average power supplied to the output stage can be controlled. This in turn regulates the output voltage V_o for a given load current I_o.

From the waveforms of Fig. 9-28*c*, it can be seen that if $I_o > V_d/Z_0$, i_T will not come back to zero naturally and the switch will have to be forced off, thus resulting in turn-off losses.

Zero-current switching can also be obtained by connecting C_r in parallel with D as shown in Fig. 9-30*a*. As discussed previously, i_o can be assumed to be a current of constant magnitude I_o in Fig. 9-30*a* during a high-frequency resonant cycle.

Initially both the capacitor voltage (across C_r) and the inductor current (through L_r) are assumed to be zero and the load current I_o freewheels through the diode D. The converter operation can be divided into the following intervals for which the converter waveforms as well as the corresponding circuit states are shown in Fig. 9-30*b* and 9-30*c*:

1. *Time interval* 1 *(between* t_0 *and* t_1*).* At time t_0, the switch is turned on. Because of I_o flowing through the diode it appears as a short circuit and the entire input voltage V_d appears across L_r. Therefore, the switch current builds up linearly until it becomes equal to I_o at time t_1. Beyond this time, the diode turns off and the voltage clamp across C_r is removed.
2. *Time interval* 2 *(between* t_1 *and* t_2*).* Beyond t_1, $i_T > I_o$ and their difference ($i_T - I_o$) flows through C_r. At t_1', i_T peaks and $v_c = V_d$. At time t_1'', the switch current drops from its peak value to I_o and the capacitor voltage reaches $2V_d$. The switch current eventually drops to zero at t_2 and cannot reverse through the switch (if a BJT or a MOSFET is used as a switch, then a diode in series with it must be used to block a negative voltage and to prevent the flow of reverse current through the switch). Thus, the switch current is commutated off naturally and the gate/base drive from the switch should be removed at this point.
3. *Time interval (between* t_2 *and* t_3*).* Beyond the time t_2 with the switch off, the capacitor C_r discharges into the output load and the capacitor voltage linearly drops to zero at t_3.
4. *Time interval* 4 *(between* t_3 *and* t_4*).* Beyond t_3, the load current just freewheels through the diode until a time t_4, when the switch is turned on and the next switching cycle begins. This time interval is controlled to adjust the output voltage.

Under a steady-state operating condition, the average voltage across the filter inductor is zero; therefore the voltage across C_r averaged over one switching cycle equals the output voltage V_o. By controlling the freewheeling time interval 4 (i.e., by controlling the switching frequency), the output voltage V_o can be regulated.

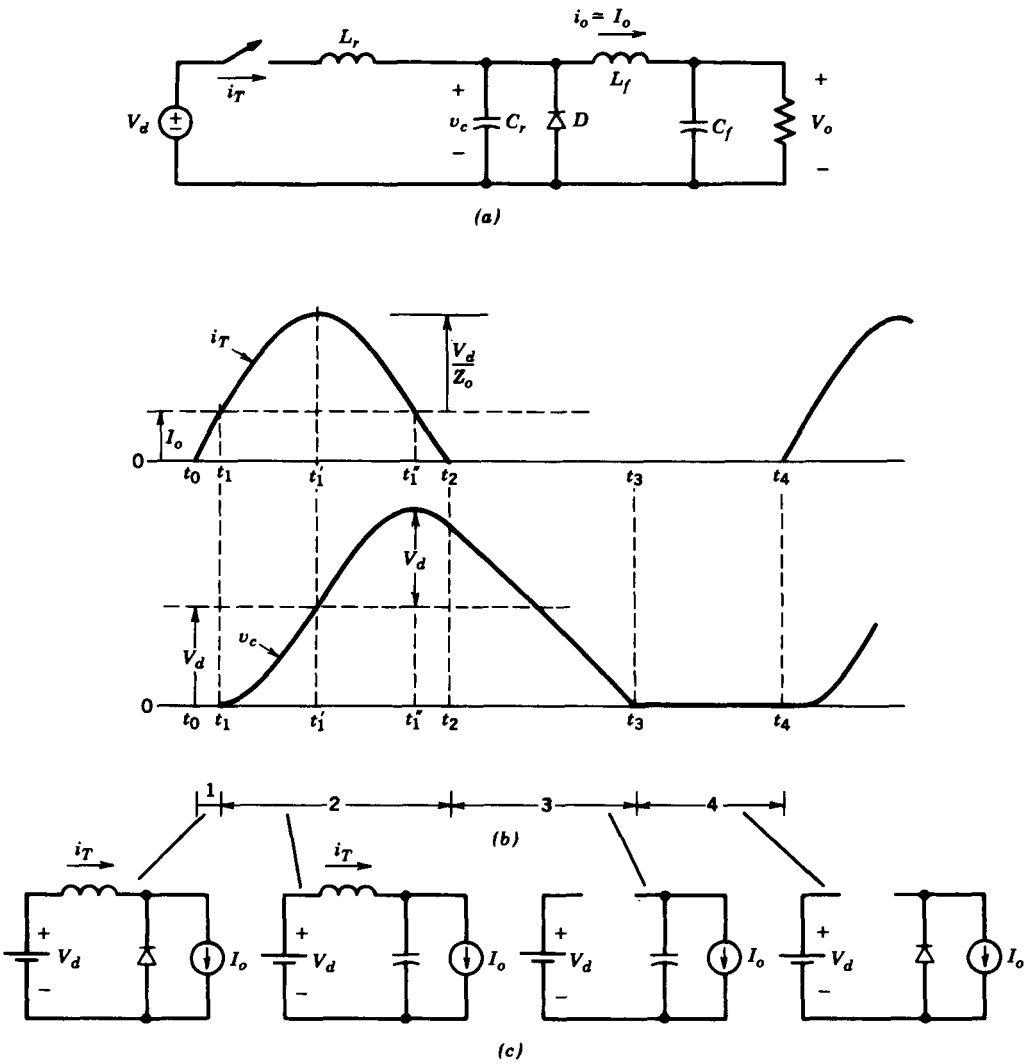


Figure 9-30 ZCS resonant-switch dc–dc converter; alternate configuration.

From the waveforms of Fig. 9-30*b*, the following circuit properties can be observed:

- The L_r and C_r together determine the natural resonance frequency $\omega_0 = 1/(2\pi\sqrt{L_rC_r})$, which can be made to be large (in the megahertz range) by proper selection of L_r and C_r. Both the switch turn-on and turn-off occur at zero current, thus reducing the switching losses. It should be noted that at turn-on, the voltage across the switch equals V_d. This results in losses, as discussed in Section 9-5-3.
- The load current I_o must be less than a maximum value of V_d/Z_0, which depends on the circuit parameters. Otherwise, the switch would have to turn off a finite amount of current.
- At a given switching frequency of operation, V_o declines with increasing load. Therefore, the switching frequency ω_s must be increased to regulate V_o. The opposite is true if the load decreases.

- By placing a diode in the antiparallel across the switch in Fig. 9-30*a*, the inductor current is allowed to reverse. This permits excess energy in the resonant circuit at light loads to be transferred back to the voltage source V_d. This significantly reduces the dependence of V_o on the output load.

Since the switching losses are minimized and the EMI is reduced, very high switching frequencies can be attained. One drawback of such a converter is that the switch peak current rating required is significantly higher than the load current. This also implies that the conduction losses in the switch would be higher compared with its switch-mode counterpart. In references 25 and 26, it has been shown that this principle can be applied to various other single-switch dc–dc converter topologies.

9-5-2 ZVS RESONANT-SWITCH CONVERTERS

In these converters, the resonant capacitor produces a zero voltage across the switch, at which instant the switch can be turned on or off. Such a step-down dc–dc converter circuit is shown in Fig. 9-31*a*, where a diode D_r is connected in antiparallel with the switch. As discussed previously, the output current i_o can be assumed to be a current of constant magnitude I_o in Fig. 9-31*a* during a high-frequency resonant cycle.

Initially, the switch is conducting I_o and therefore, $I_{L0} = I_o$ and $V_{c0} = 0$. The converter operation can be divided into the following intervals for which the converter waveforms as well as the corresponding circuit states are shown in Fig. 9-31*b* and 9-31*c*, respectively:

1. *Time interval* 1 *(between* t_0 *and* t_1*).* At time t_0, the switch is turned off. Because of C_r, the voltage across the switch builds up slowly but linearly from zero *to* V_d at t_1. This results in a zero-voltage turn-off of the switch.
2. *Time interval 2 (between* t_1 *and* t_2*).* Beyond t_1, since $v_c > V_d$, the diode D becomes forward biased, C_r and L_r resonate, and the analysis of Section 9-3-1-1 applies. At t_1', i_L goes through zero and v_c reaches its peak of $V_d + Z_0 I_o$. At t_1'', $v_c = V_d$ and $i_L = -I_o$. At t_2, the capacitor voltage reaches zero and cannot reverse its polarity because the diode D_r begins to conduct.

   Note that the load current I_o should be sufficiently large so that $Z_0 I_o > V_d$. Otherwise, the switch voltage will not come back to zero naturally and the switch will have to be turned on at a nonzero voltage, resulting in turn-on losses (the energy stored in C_r will dissipate in the switch).
3. *Time interval* 3 *(between* t_2 *and* t_3*).* Beyond t_2, the capacitor voltage is clamped to zero by D_r, which conducts the negative i_L. The gate drive to the switch is applied once its antiparallel diode begins to conduct. Now i_L increases linearly and goes through zero at time t_2', at which instant i_L begins to flow through the switch. Therefore, the switch turns on at a zero voltage and zero current. Here i_L increases linearly to I_o at t_3.
4. *Time interval 4 (between* t_3 *and* t_4*).* Once i_L reaches I_o at t_3, the freewheeling diode D turns off. Because a small negative slope is associated with *di/dt* through the diode at turn-off, there are no diode reverse-recovery problems like the ones encountered in the switch mode. The switch conducts I_o as long as it is kept on until t_4. The interval $t_4 - t_3$ can be controlled. At t_4, the switch is turned off and the next cycle ensues.

It is clear from the waveforms of Fig. 9-31*b* that the switch current is limited to I_o. The voltage v_{oi} across the output diode as defined in Fig. 9-31*a*, is plotted in Fig. 9-32.

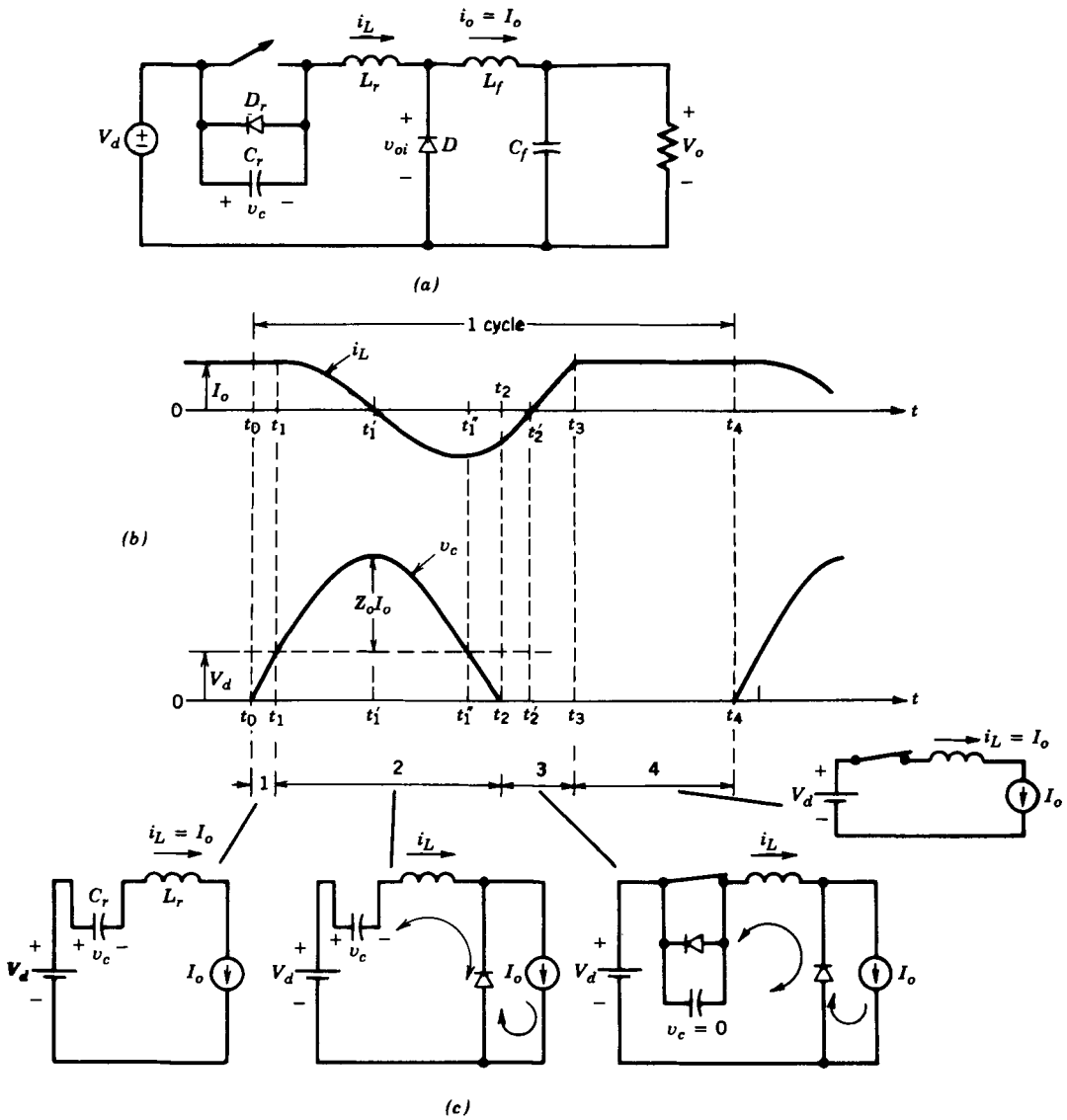


Figure 9-31 ZVS resonant-switch dc–dc converter.

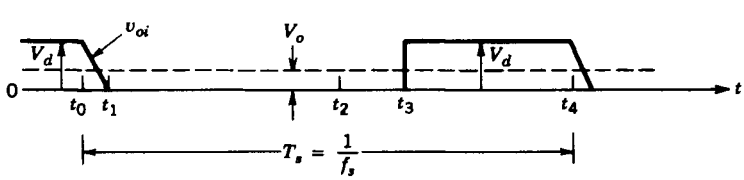


Figure 9-32 The v_{oi} waveform in a ZVS resonant-switch dc–dc converter.

By controlling the on interval $t_4 - t_3$ of the switch, the average value of v_{oi} and, hence, the average power supplied to the output stage can be controlled. This in turn regulates the output voltage V_o for a given load current I_o.

This zero-voltage-switching approach can also be applied to various other single-switch dc–dc converter topologies, as described in reference 27.

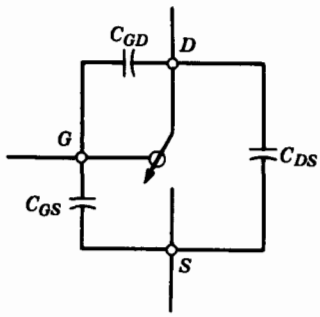


Figure 9-33 Switch internal capacitances.

9-5-3 COMPARISON OF ZCS AND ZVS TOPOLOGIES

Both of these techniques require a variable-frequency control to regulate the output voltage.

In the ZCS, the switch is required to conduct a peak current that is higher than the load current I_o by an amount V_d/Z_0. For natural turn-off of the switch at zero current, the load current I_o must not exceed V_d/Z_0. Therefore, there is a limit on how low the load resistance can become. By placing a diode in antiparallel with the switch, the output voltage can be made insensitive to the load variations.

In the ZVS topology discussed here, the switch is required to withstand a forward voltage that is higher than V_d by an amount $Z_0 I_o$. For zero-voltage (lossless) turn-on of the switch, the load current I_o must be greater than V_d/Z_0. Therefore, if the output load current I_o varies in a wide range, then the foregoing two conditions result in a very large voltage rating of the switch (see Problem 9-13). Therefore, this technique is limited to an essentially constant load application. To overcome this limitation, a zero-voltage-switching multiresonant technique is described in reference 29.

In general, ZVS is preferable over ZCS at high switching frequencies. The reason has to do with the internal capacitances of the switch, as shown in Fig. 9-33. When the switch turns on at zero current but at a finite voltage, the charge on the internal capacitances is dissipated in the switch. As discussed in reference 30, this loss becomes significant at very high switching frequencies. However, no such loss occurs if the switch turns on at a zero voltage.

9-6 ZERO-VOLTAGE-SWITCHING, CLAMPED-VOLTAGE TOPOLOGIES

In the literature, these topologies have been referred to as the pseudo-resonant- and resonant-transition topologies. In these topologies, the switches turn on and turn off at zero voltage. But unlike the ZVS topology discussed in Section 9-5-2, the peak voltage of a switch is clamped at the input dc voltage. Such converters consist of at least one converter leg having two switches.

9-6-1 ZVS-CV dc–dc CONVERTERS

The basic principle is shown by means of the dc–dc step-down converter shown in Fig. 9-34*a*, consisting of two switches. The filter inductor L_f is very small compared with the normal switch-mode topology so that i_L becomes positive as well as negative during each

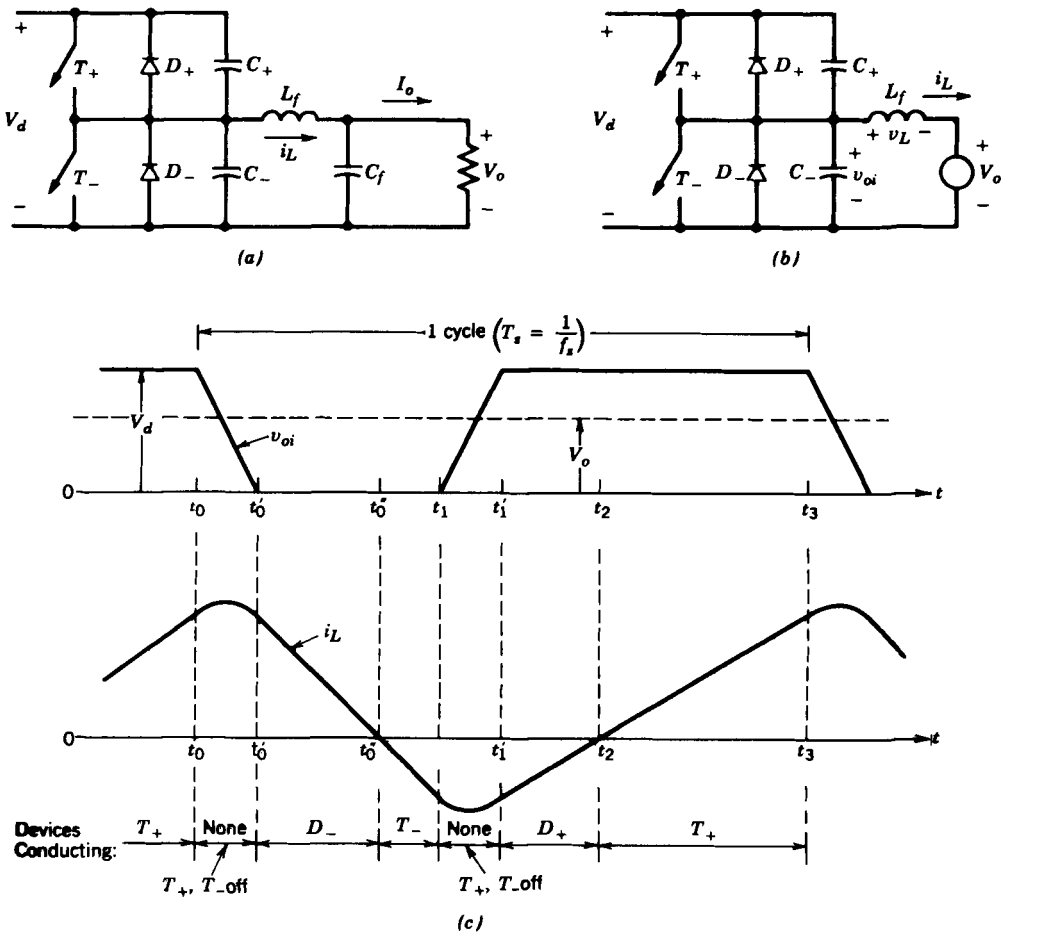


Figure 9-34 ZVS-CV dc–dc converter.

cycle of operation. Assuming C_f to be large, the filter capacitor and the load can be replaced by a dc voltage V_o in steady state as shown in the equivalent circuit of Fig. 9-34*b*. The waveforms are shown in Fig. 9-34*c*.

Initially, T_+ is conducting a positive i_L and v_L ($=V_d - V_o$) is positive. At time t_0, T_+ is turned off at zero voltage because of C_+ in Fig. 9-34*a*; the voltage across T_+ builds up slowly compared with its switching time. With T_- off and T_+ just off, the subcircuit is as shown in Fig. 9-35*a*. It can be redrawn as in Fig. 9-35*b*, where the initial voltage vV_d on C_- is shown explicitly by means of a voltage source. Since $C_+ = C_- = \frac{1}{2}C$, the Thévenin equivalent of the circuit on the left results in the circuit of Fig. 9-35*c*. Since C is very small, the resonant frequency $f_0 = 1/(2\pi\sqrt{L_f C})$ is much larger than the switching frequency of the converter. Moreover, $Z_0 = \sqrt{L_f/C}$ in this circuit is very large, resulting in a small variation in i_L during the time interval shown in Fig. 9-35*d*. At t_0', v_{oi}, the voltage across C_-, reaches zero, beyond which time this subcircuit has to be modified since v_{oi} cannot become negative because of the presence of D_- in the original circuit. During the time interval t_0'–t_0, the magnitude of dv/dt across both the capacitors is the same; therefore, $\frac{1}{2}i_L$ flows through each of the capacitors during this interval since $C_+ = C_-$.

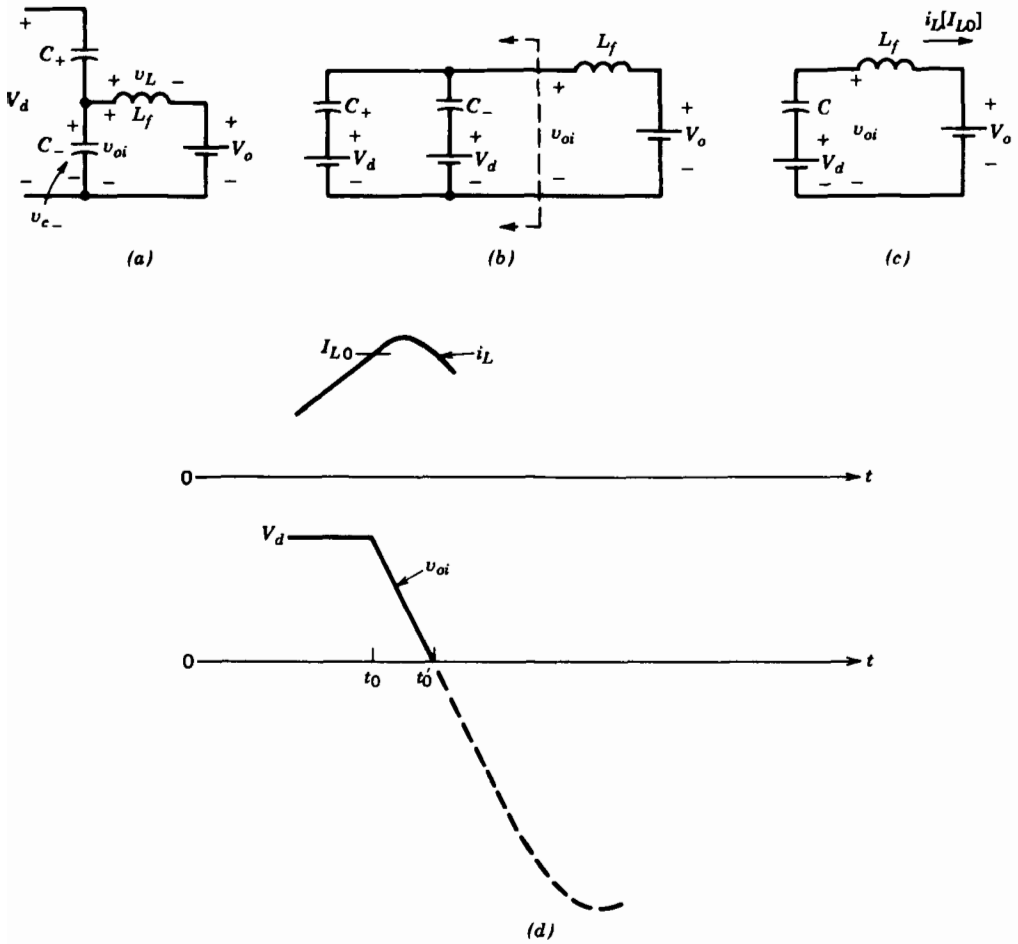


Figure 9-35 ZVS-CV dc–dc converter; T_+, T_- off.

The preceding discussion can be simplified if i_L during this interval is assumed to be essentially constant. This allows the assumption that v_{oi} changes linearly, as shown in Fig. 9-34*c* during the blanking-time interval where both the switches are off.

Beyond t_0', i_L decreases linearly, since it flows through D_-, and therefore, $v_L = -V_o$. Once D_- begins to conduct, T_- is gated on. At t_0'', i_L reverses direction and flows through T_-.

At t_1, T_- is turned off at zero voltage and after a capacitor charging–discharging interval t_1'–t_1, similar to t_0' to t_0, the negative i_L flows through D_+. Since v_L $(=V_d - V_o)$ is positive beyond t_1', i_L increases. Here T_+ is gated on at zero voltage as soon as D_+ begins to conduct. At t_2, i_L becomes positive and flows through T_+.

At t_3, T_+ is turned off at zero voltage, thus completing a cycle with a time period $T_s = (t_3 - t_0)$.

As shown by the waveforms in Fig. 9-34*c*, the switch voltage peak in this topology is clamped at V_d.

An important observation is that for the zero-voltage turn-off of a switch, a capacitor is connected directly across the switch. Therefore, the switch must be turned on only at zero voltage; otherwise the energy stored in the capacitor will be dissipated in the switch. Therefore, the diode in antiparallel with the switch must conduct prior to the closing of

the switch. This requires that in the circuit of Fig. 9-34*a*, i_L must flow in both directions during each cycle to satisfy this requirement for both the switches.

In such a circuit, the output voltage can be regulated by means of a constant-switching-frequency PVM control. Assuming the blanking-time intervals $t_0'-t_0$ and $t_1'-t_1$, during which the resonant transition occurs, to be much smaller than the time period T_s of the switching frequency, the voltage v_{oi} in Fig. 9-34*c* is of a rectangular waveform. Since the average voltage across L_f is zero, the average value of v_{oi} equals V_o. Therefore, $V_o = DV_d$, where D is the duty ratio of the switch T_+ and DT_s is the time interval during which either T_+ or D_+ is conducting. The average value of i_L equals the output current I_o.

If a constant-frequency PWM control is used to regulate V_o, then L_f needs to be chosen such that even under the minimum value of V_d and the highest load (i.e., the minimum load resistance), i_L reaches a value less than zero.

The advantage of this ZVS-CV is that the switch voltages are clamped to V_d. The disadvantage is that because of the higher ripple in i_L, the switches need to carry higher peak currents as compared to the switch mode of operation.

9-6-2 ZVS-CV dc-TO-ac INVERTERS

It should be noted that the dc–dc converter discussed in Section 9-6-1 is capable of a two-quadrant operation where i_o can reverse. Therefore, such a converter can be modified as shown in Fig. 9-36*a*, which results in a half-bridge square-wave dc-to-ac inverter to supply an inductive load. The resulting waveforms with equal switch duty ratios are shown in Fig. 9-36*b*, and the switching losses are eliminated, since the switches turn on and turn off at zero voltage. The load current must lag the voltage (i.e., the load must be inductive like a motor load) for the switchings to occur at a zero voltage.

It is possible to operate the inverter of Fig. 9-36*a* in a current-regulated mode, similar to that discussed in Chapter 8. However, to achieve zero-voltage switchings, both switches must conduct every switching cycle, and therefore i_o must flow in each direction during every switching cycle. The waveforms for square-wave and PWM modes are shown in Figs. 9-36*b* and 9-36*c*, respectively. This concept can be extended to a three-phase inverter as shown in Fig. 9-37.

9-6-3 ZVS-CV dc–dc CONVERTER WITH VOLTAGE CANCELLATION

The ZVS-CV technique can be extended to the single-phase dc-to-ac inverter with voltage cancellation. The switch-mode circuit, which was discussed in detail in Chapter 8, is shown in Fig. 9-38*a*, and the resulting waveforms are shown in Fig. 9-38*b*, where both switches in each leg operate at a 50% duty ratio but the phase delay ϕ between the outputs of the two legs is controlled in order to control the output v_{AB} of the full bridge. The output voltage of the full bridge is stepped down through an isolation transformer and then rectified to yield an overall dc–dc converter.

The switch-mode circuit of Fig. 9-38*a* can be modified to provide ZVC-CV by adding L_A, C_A+, C_{A-} to leg A and L_B, C_{B+}, C_{B-} to leg B, as shown in Fig. 9-39*a*. For simplicity, the transformer is replaced by its magnetizing inductance L_m and its leakage inductance is neglected. The output stage is represented by the output current I_o. The resulting waveforms are shown in Fig. 9-39*c*, where the idealized switch-mode waveforms of Fig. 9-38 are repeated in Fig. 9-39*b* for comparison. Proper selection of inductance and capacitance values and a proper switching strategy result in a ZVS-CV switching, as discussed in reference 34.

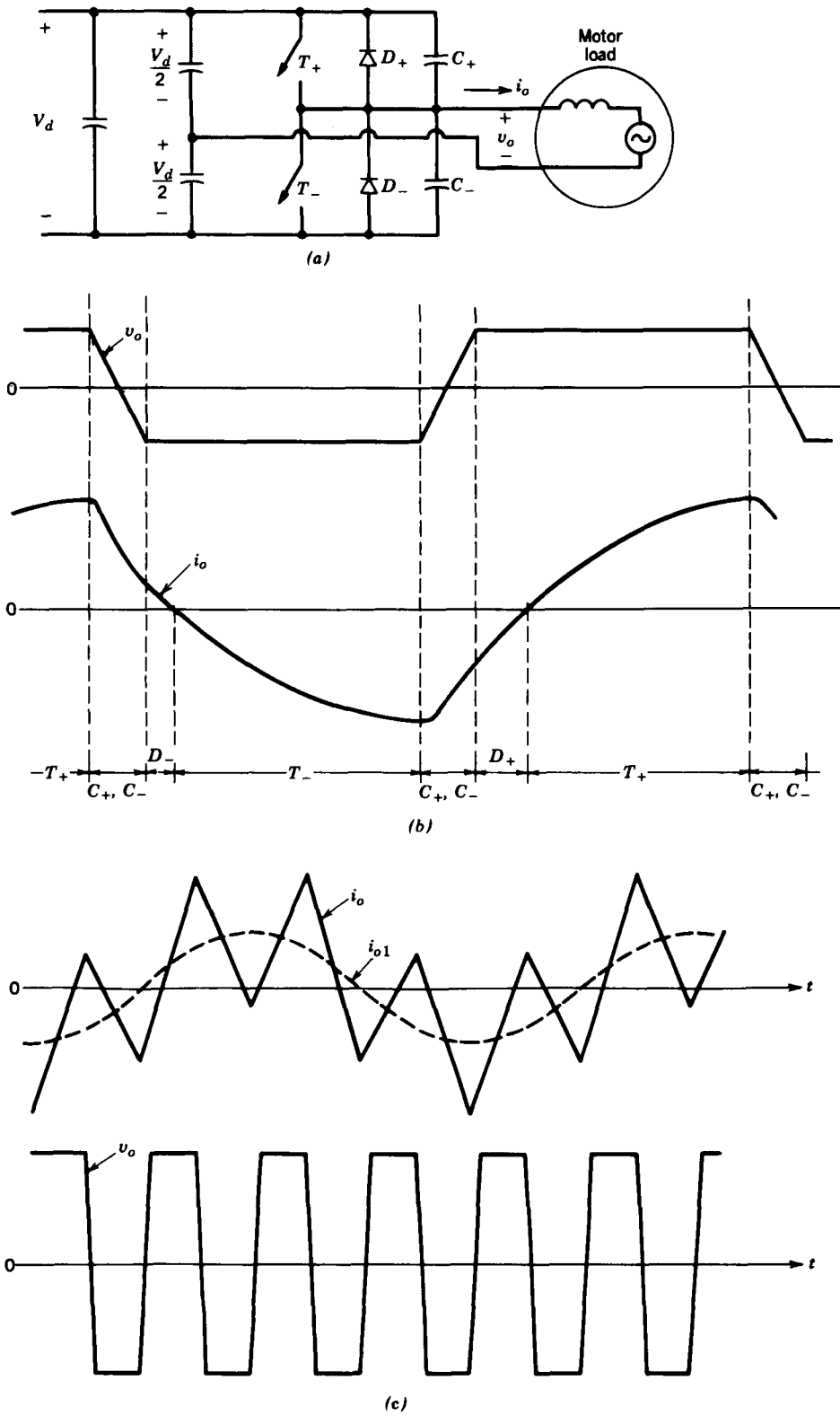


Figure 9-36 ZVS-CV dc-to-ac inverter: (*a*) half-bridge; (*b*) square-wave mode; (*c*) current-regulated mode.

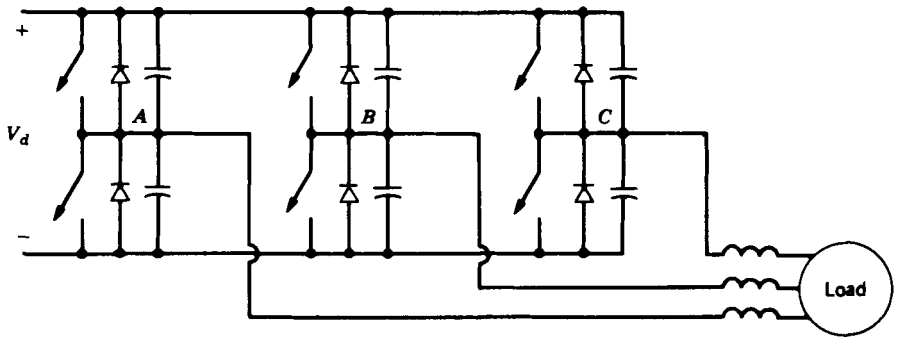
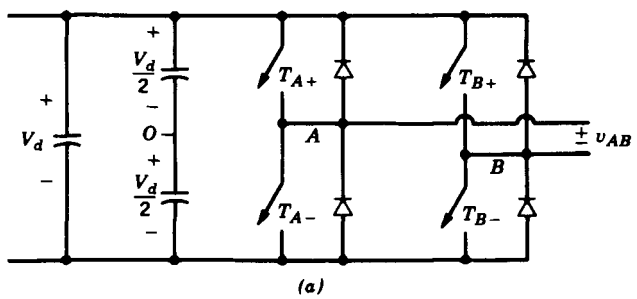
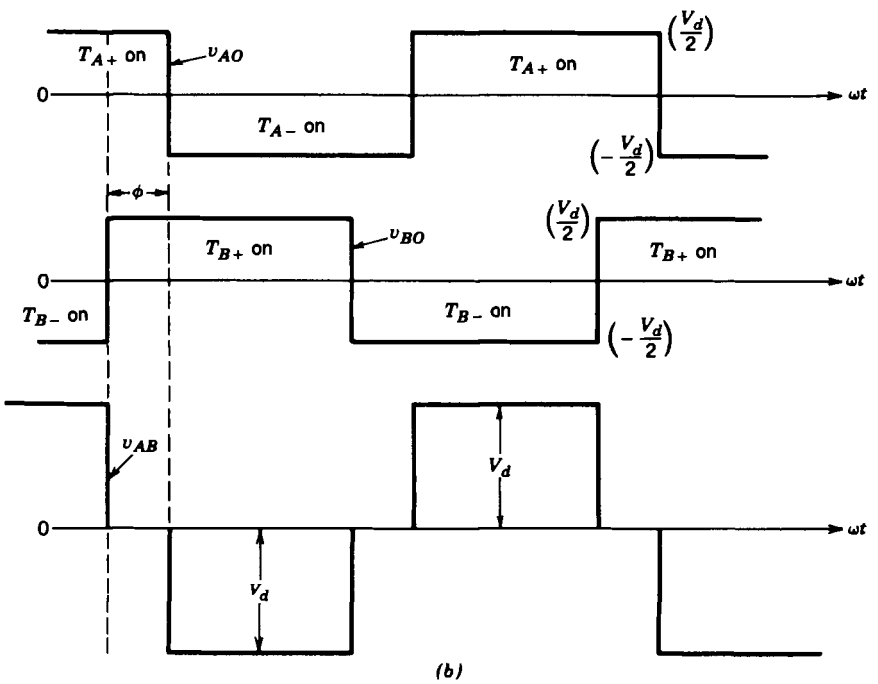


Figure 9-37 Three-phase, ZVS-CV dc-to-ac inverter.



(a)



(b)

Figure 9-38 Voltage control by voltage cancellation: conventional switch-mode converter.

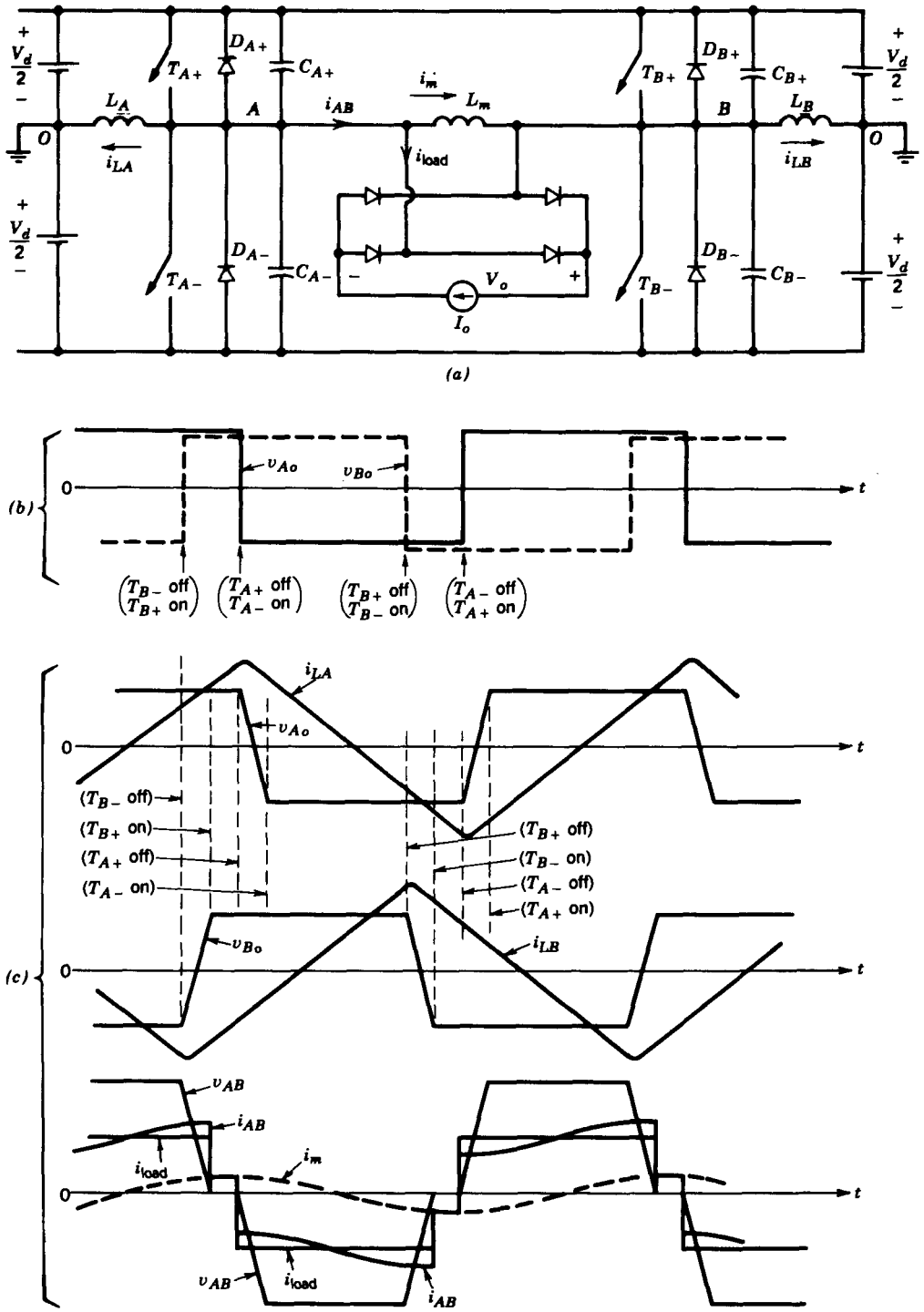


Figure 9-39 ZVS-CV full-bridge dc–dc converter: (*a*) circuit; (*b*) idealized switch-mode waveforms; (*c*) ZVS-CV waveforms.

9-7 RESONANT-dc-LINK INVERTERS WITH ZERO-VOLTAGE SWITCHINGS

In the conventional switch-mode PWM inverters of the type discussed in Chapter 8, the input is a dc voltage. To avoid the switching losses in the inverter, a new topology has been recently proposed in reference 35, where a resonant circuit is introduced in between the dc input voltage and the PWM inverter. As a result, the input voltage to the inverter in the basic configuration oscillates between zero and slightly greater than twice the dc input voltage. The inverter switches are turned on and turned off at zero voltage.

The basic concept is illustrated by means of the circuit of Fig. 9-40*a*. The resonant circuit consists of L_r, C_r, and a switch with an antiparallel diode. The load of

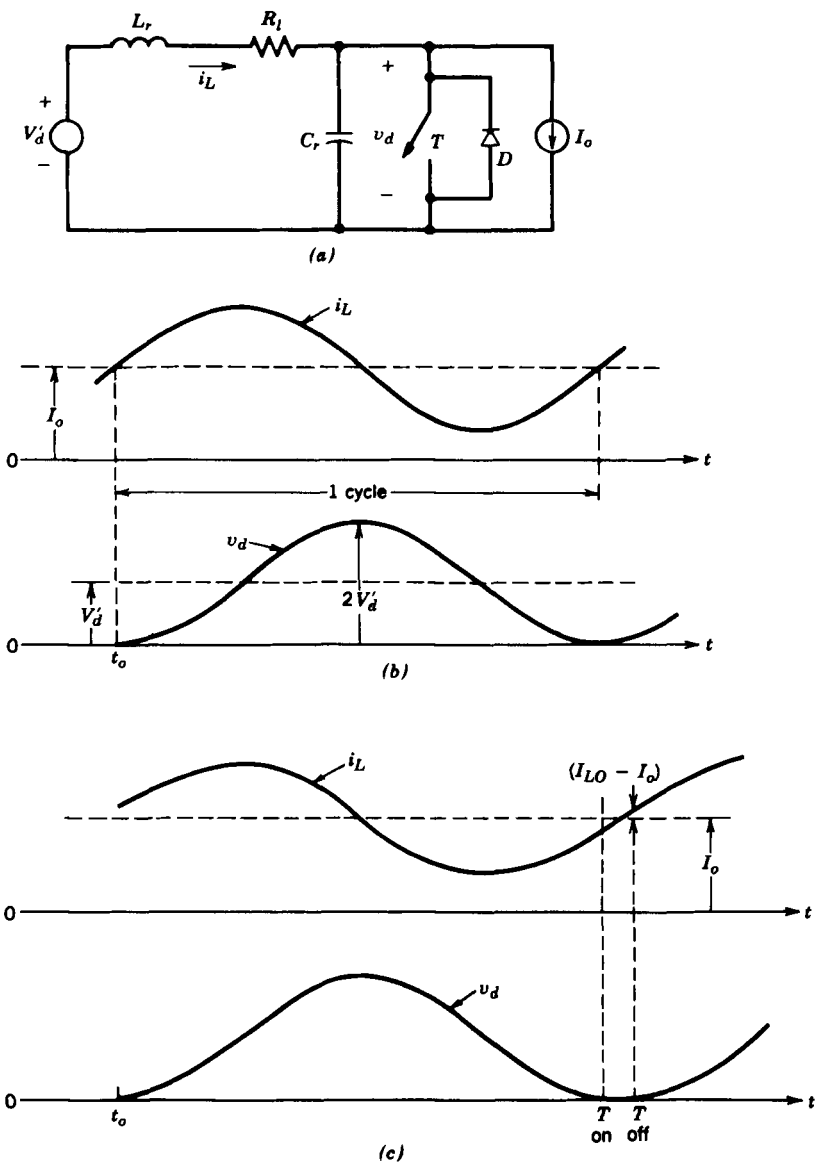


Figure 9-40 Resonant-dc-link inverter, basic concept: (*a*) basic circuit; (*b*) lossless $R_l = 0$; (*c*) losses are present.

the circuit is represented by a current I_o, which represents, for example, the current being supplied by the inverter to a motor load. Because of the internal inductance of the load, it is reasonable to assume I_o to be constant in magnitude during a resonant frequency cycle.

As a first step, R_l is assumed to be zero. Initially, the switch is closed and the difference of i_L and I_o flows through the diode–switch combination. Current i_L builds up linearly. At time t_0, with $i_L = I_{L0}$, the switch is turned off at zero voltage. The equations for the resonant circuit are as follows for $t > t_0$:

$$i_L(t) = I_o + \left[\frac{V_d'}{\omega_0 L_r}\sin \omega_0(t - t_0) + (I_{L0} - I_o)\cos \omega_0(t - t_0)\right] \tag{9-34}$$

and

$$v_d(t) = V_d' + [\omega_0 L_r(I_{L0} - I_o)\sin \omega_o t - V_d' \cos \omega_0 t] \tag{9-35}$$

where

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} \tag{9-36}$$

The waveforms in Fig. 9-40*b* for $I_{L0} = I_o$ show that v_d returns to zero and i_L returns to I_o after one resonant cycle from the switch opening. Therefore, in this idealized circuit without any losses, the switch T and diode D can be removed once the oscillations start.

In the basic circuit of Fig. 9-40*a*, R_l represents the losses. In order for the zero-voltage turn-on and turn-off of the switch to occur, v_d must return to zero. In the presence of losses in R_l, I_{L0} must be greater than I_o at the instant the switch is turned off. The waveforms are shown in Fig. 9-40*c*. If the switch is kept on too long and I_{L0} is much larger than I_o, then v_d will peak at a value significantly larger than $2V_d'$. Therefore, $I_{L0} - I_o$ must be controlled by controlling the time interval during which the switch remains closed.

The foregoing concept can be applied to the three-phase PWM inverter of Fig. 9-41. The resonant switch T and D of Fig. 9-40*a* are not needed since their function can be fulfilled by any of two switches comprising an inverter leg. The switches in any of the three inverter legs can be turned on and turned off at zero voltage when v_d reaches zero.

Further modifications to clamp the peak voltage across the switches to less than twice the input dc voltage have been discussed in the literature.

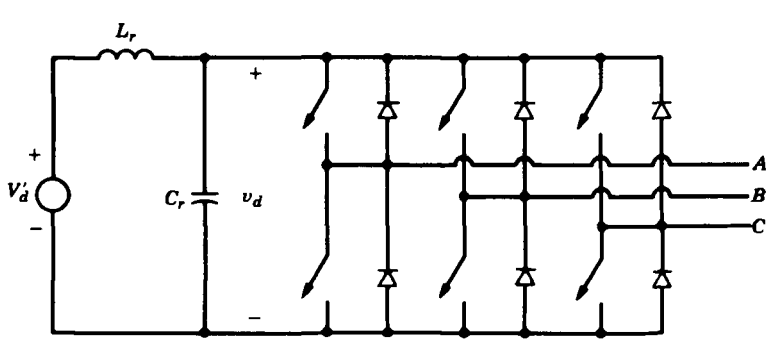


Figure 9-41 Three-phase resonant-dc-link inverter.

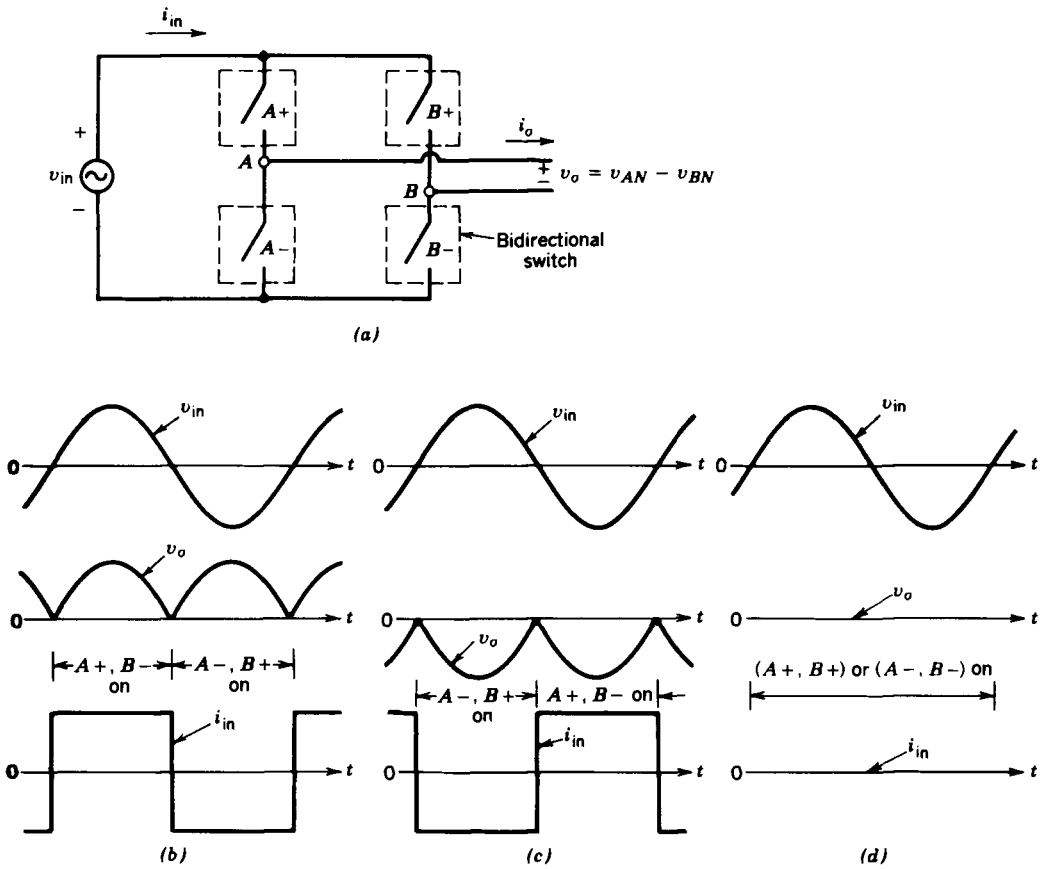


Figure 9-42 High-frequency-link integral-half-cycle inverter.

9-8 HIGH-FREQUENCY-LINK INTEGRAL-HALF-CYCLE CONVERTERS

Unlike the resonant-dc-link converters where the input to the single-phase or three-phase converter oscillates between zero and a value higher than the average input dc voltage, in the high-frequency-link converters the input to the single-phase or three-phase converter is a single-phase, high-frequency sinusoidal ac, as shown in Fig. 9-42*a*. As discussed in reference 38, by turning the inverter switches on or off when the input voltage passes through zero, the switching losses can be minimized.

Figure 9-42*a* shows a single-phase converter of this type with a high-frequency sinusoidal input voltage v_{in}. The output is synthesized to be a low-frequency ac, for example, to supply a motor load. This requires that all four switches be bidirectional. Each bidirectional switch in Fig. 9-42*a* can be obtained by connecting two unidirectional switches with reverse blocking capability in antiparallel.

To describe the operating principle, the output load current is assumed to be a constant I_o during a cycle of high-frequency ac input. Here I_o can be positive or negative. For either direction of I_o, v_{AB} can consist of two positive half-cycles, two negative half-cycles, or zero (or any combination of these three options). These three options and

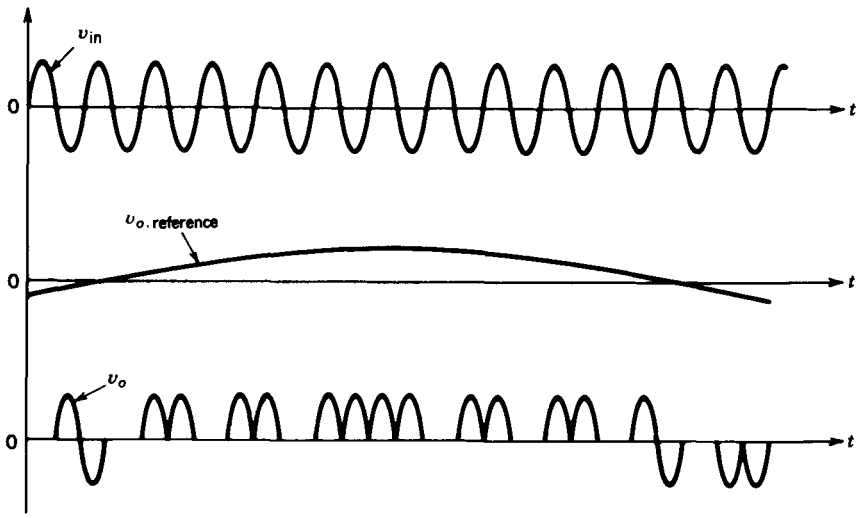


Figure 9-43 Synthesis of low-frequency ac output.

the corresponding i_{in} are shown in Fig. 9-42*b* through 9-42*d* for a positive I_o, for example. This control over v_o to be positive, negative, or zero during each high-frequency half-cycle allows a low-frequency output to be synthesized to be of the desirable frequency and magnitude, as shown in Fig. 9-43. This control is discussed in detail in reference 38. Since the low-frequency output consists of an integral number of half-cycles of the high-frequency input, these converters are labeled high-frequency-link integral-half-cycle converters.

This concept can also be extended to deliver three-phase ac output by the circuit of Fig. 9-44. It should be noted that in both the single-phase and three-phase converters, a parallel-resonant filter of the type shown in Fig. 9-44 must be used. It is tuned to be parallel resonant at the input voltage frequency f_{in}. Therefore, it does not draw any current from the high-frequency ac input. However, the capacitor C_f provides a low-impedance path to all other frequency components in i_{in} so that they do not have to be supplied by v_{in} through the stray inductance L_{stray}.

The low-frequency output may in fact be dc in the circuit of Fig. 9-42*a*. Also, the power can flow in either direction in these converters.

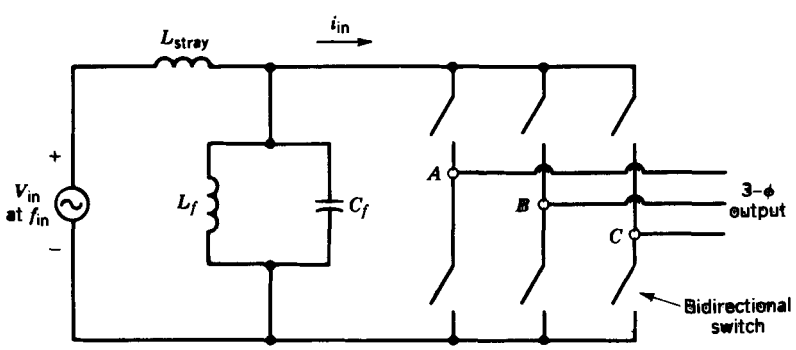


Figure 9-44 High-frequency ac to low-frequency three-phase ac converter.

These high-frequency-link converters are a form of cycloconverters, whereby the power is transferred between two ac systems operating at two different frequencies without an intermediate dc link. Unlike the phase-controlled, line-frequency cycloconverters using thyristors, which are described in Chapter 15, the bidirectional controllable switches in these high-frequency-link converters are turned on or off when the input high-frequency ac passes through zero.

SUMMARY

In this chapter, various techniques are discussed that can either eliminate or diminish the stresses and the switching losses in the semiconductor devices. The following converters are described:

1. Load-resonant converters
   (a) Series-loaded resonant (SLR) dc–dc converters
   (b) Parallel-loaded resonant (PLR) dc–dc converters
   (c) Hybrid-resonant, dc–dc converters
   (d) Current-source, parallel-resonant dc-to-ac inverters for induction heating
   (e) Class E converters
2. Resonant-switch converters
   (a) Zero-current-switching (ZCS) converters
   (b) Zero-voltage-switching (ZVS) converters
   (c) Zero-voltage-switching, clamped-voltage (ZVS-CV) converters
      (i) ZVS-CV dc–dc converters
      (ii) ZVS-CV dc-to-ac inverters
      (iii) ZVS-CV dc–dc converters with zero voltage cancellation
3. Resonant-dc-link inverters with zero-voltage switchings
4. High-frequency-link integral-half-cycle converters

An overview of these converters is provided in reference 41.

PROBLEMS

SLR dc–dc CONVERTERS

9-1 The SLR dc–dc converter of Fig. 9-10*a* is operating in a discontinuous-conduction mode with $\omega_s < 0.5\omega_0$. In the waveforms of Fig. 9-11 (with $t_0 = 0$), the initial conditions in terms of normalized quantities are always as follows: $V_{c0} = -2V_o$ and $I_{L0} = 0$. Show that in terms of normalized quantities, $V_{c,\text{peak}} = 2$ and $I_{L,\text{peak}} = 1 + V_o$.

9-2 Design an SLR dc–dc converter of Fig. 9-10*a* with an isolation transformer of turns-ratio n : 1, where $V_d = 155$ V, and the operating frequency $f_s = 100$ kHz. The output is at 5 V and 20 A.

(a) The foregoing converter is to operate in a discontinous-condution mode with $\omega_s < 0.5\omega_0$. The normalized output voltage V_o is chosen to be 0.9 and the normalized frequency to be 0.45. Using the curves of Fig. 9-15, obtain turns ratio n, L_r, and C_r.

(b) Obtain the numerical value for the sum of peak energies stored in L_r and C_r:

$$S = \tfrac{1}{2}L_r I_{L,\text{peak}}^2 + \tfrac{1}{2}C_r V_{c,\text{peak}}^2$$