Chapter 6

THE EVENT MANAGERS (EVA, EVB)

This chapter explains the features and operation of the LF2407 Event Managers (EV1, EV2). There are two identical event managers on board the LF2407 DSP. All control orientated features of the LF2407 are centered in the EV. The event manager peripheral is made up of components such as timers and pulse width modulation (PWM) generators. We start with a brief overview of the EV without getting into too much detail. Since the EV consists of several sub-components, we discuss in detail the operation and functionality of each sub-component separately in subsequent sections.

6.1 Overview of the Event Manager (EV)

We start with the EV by reviewing the multiple functional modules of the peripheral. The two EVs (EVA/B) are identical to one another in terms of functionality and register/bit definition, but have different register names and addresses. Since both EV1 and EV2 are identical, only the functionality of EV1 will be explained.

Each EV module in the LF2407 contains the following sub-components:

- Interrupt logic
- Two general-purpose (GP) timers
- Three compare units
- PWM circuits that include space vector PWM circuits, dead-band generation units, and output logic
- Three Capture Units
- Quadrature encoder pulse (QEP) circuit

Figure 6.1 shows a block diagram of the EVA module. Similarly, Fig. 6.2 illustrates the block diagram of EVB.

Like all peripherals, the EV registers occupy a range of 16-bit memory addresses in data memory space. Most of these registers are programmable control and data registers, but read-only status registers are also present. EVA registers are located in the data memory range 7400h to 7431h. EVB registers are located in the range of 7500h to 7531h. Some of the EV memory allocation range is for use by the DSP only. These undefined registers and undefined bits of EV registers will just read zero when read by user software. Writes also have no effect on these registers. As a general rule, one should not write to reserved or illegal addresses in order to avoid an illegal address non-maskable interrupt (NMI) from occurring.

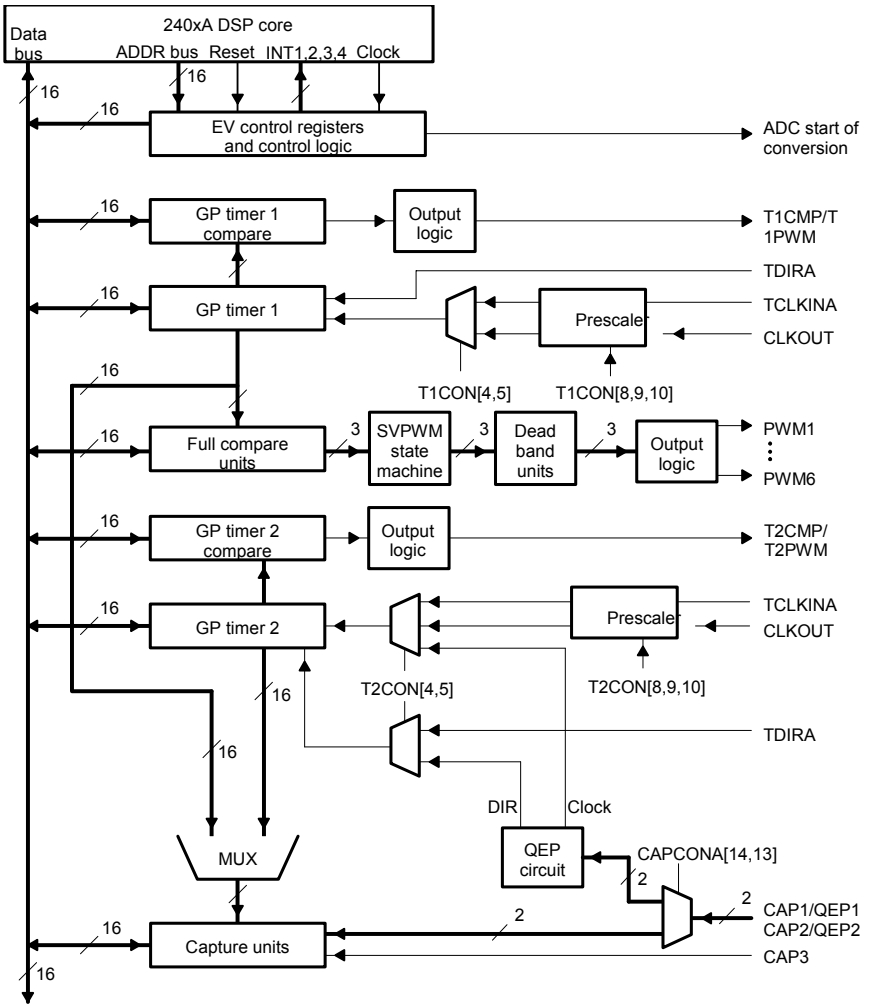

Figure 6.1 Event Manager A (EVA) block diagram. (Courtesy of Texas Instruments)

6.2 Event Manager Interrupts

The interrupt system in the EV will be discussed first because each of the sub-modules of the EVs have interrupt flags. The EV interrupt sub-system is slightly different from that of the main interrupt system. Each EV has its own "local" interrupt sub-system which includes its own interrupt mask and flag registers. After the EV interrupts pass through the sub-system, they flow into the PIE just like any other interrupt on the LF2407. The EV interrupts are arranged into three groups (A, B, C). Each group (A,B,C) has its own mask and flag register and is assigned to

a particular CPU interrupt priority level at the PIE. EV interrupts happen to be only at the INT2, INT3, and INT4 CPU priority levels.

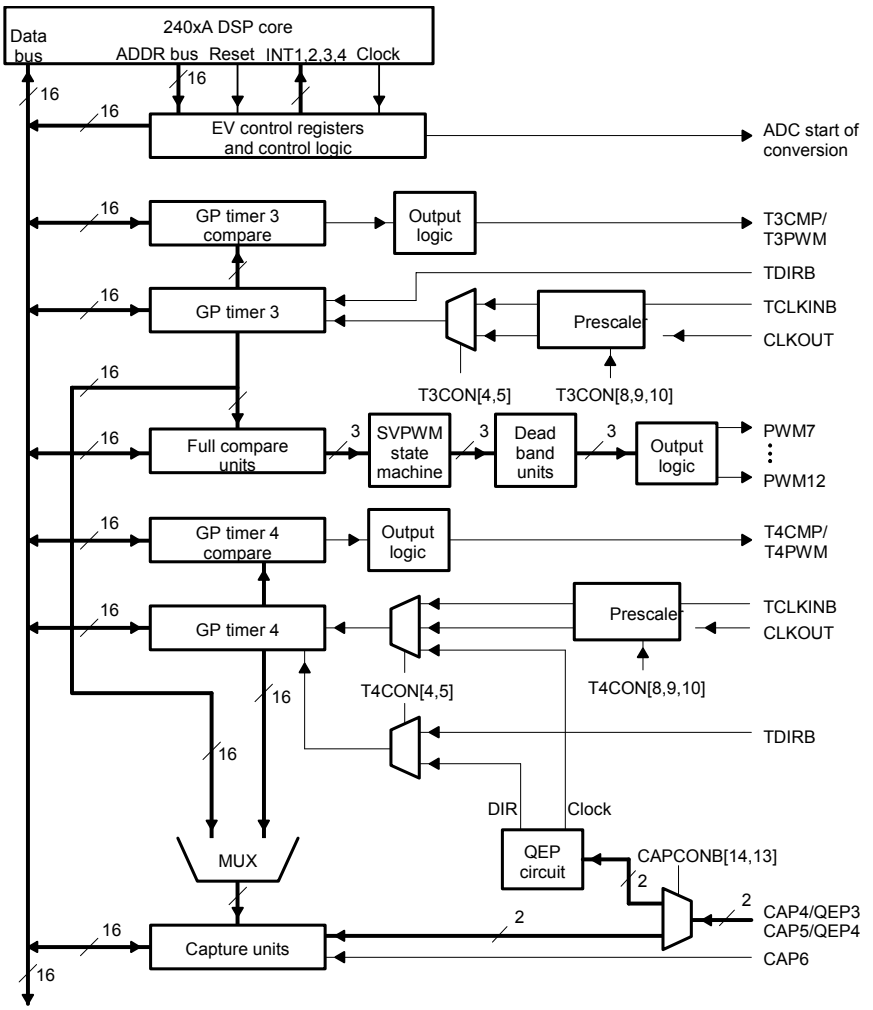

Figure 6.2 Event Manager B (EVB) block diagram. (Courtesy of Texas Instruments)

The following are the sequential steps for interrupt response within the EV:

1. ***Interrupt source***. When an EV interrupt condition occurs, the respective flag bits in registers EVxIFRA, EVxIFRB, or EVxIFRC (x = A or B) are set. As with other peripheral level flags, once set, these flags remain set until *explicitly* cleared by the software. In other words, you must clear

theses flags "manually" through your software in order for future interrupts to be recognized.

2. ***Interrupt enable.*** The EV interrupts can be individually enabled or disabled by the EV interrupt mask registers EVxIMRA, EVxIMRB, and EVxIMRC (x being either EV = A or B). To enable (unmask) an interrupt, the user must set the corresponding bit to "1". To disable (mask) the interrupt, clear the corresponding bit to "0". From now on, the interrupt is handled like other peripheral interrupts as discussed earlier in the text.

3. ***PIE request.*** If both interrupt flag bits and interrupt mask bits are set, then the interrupt request is passed to the PIE module. As with any other peripheral interrupts, the PIE module will send the CPU a request for a CPU level interrupt of the appropriate priority level based on the priority of the received interrupts.

4. ***CPU response.*** On receiving a CPU level interrupt request, the respective bit in the CPU interrupt flag register (IFR) will be set. If the corresponding interrupt mask register (IMR) bit is set and INTM bit is cleared, then the CPU recognizes the interrupt and issues an acknowledgement to the PIE module. Following this, the CPU finishes executing the current instruction and branches to the interrupt service routine via the interrupt vector. At this time, the respective IFR bit will be cleared and the INTM bit will be set disabling further interrupt recognition. The interrupt vector contains a branch instruction for the interrupt service routine. From here, the user software controls the interrupt servicing.

5. ***Interrupt software.*** The interrupt software can include two levels of response.

    a. **GISR:** The General Interrupt Service Routine (GISR) should do any context save and read the PIVR register to decide which specific interrupt occurred. Information on PIVR values and their corresponding interrupts can be found in Tables 6.1 and 6.2. Since the PIVR value for each interrupt is unique, it can be used to branch to the interrupt service routine specific to this interrupt condition.

    b. **SISR:** The Specific Interrupt Service Routine (SISR) level will normally reside as a sub-section of the GISR. After executing the interrupt specific service code, the routine should clear the interrupt flag in the EVxIFRA, EVxIFRB, or EVxIFRC that caused the serviced interrupt. Code will return the CPU to the pre-interrupt task after enabling the CPU's global interrupt bit INTM (clear INTM bit).

EVA Interrupts

Table 6.1 EVA Interrupts and Corresponding PIVR Values

Group	Interrupt	Priority within group	Vector (ID)	Description/Source	INT
	PDPINTA	1 (highest)	0020h	Power Drive Protection Interrupt A	1
A	CMP1INT	2	0021h	Compare Unit 1 compare interrupt	2
	CMP2INT	3	0022h	Compare Unit 2 compare interrupt	2
	CMP3INT	4	0023h	Compare Unit 3 compare interrupt	2
	T1PINT	5	0027h	GP Timer 1 period interrupt	2
	T1CINT	6	0028h	GP Timer 1 compare interrupt	2
	T1UFINT	7	0029h	GP Timer 1 underflow interrupt	2
	T1OFINT	8 (lowest)	002Ah	GP Timer 1 overflow interrupt	2
B	T2PINT	1 (highest)	002Bh	GP Timer 2 period interrupt	3
	T2CINT	2	002Ch	GP Timer 2 compare interrupt	3
	T2UFINT	3	002Dh	GP Timer 2 underflow interrupt	3
	T2OFINT	4	002Eh	GP Timer 2 overflow interrupt	3
C	CAP1INT	1 (highest)	0033h	Capture Unit 1 interrupt	4
	CAP2INT	2	0034h	Capture Unit 2 interrupt	4
	CAP3INT	3	0035h	Capture Unit 3 interrupt	4

EVB Interrupts

Table 6.2 EVB Interrupts and Corresponding PIVR Values

Group	Interrupt	Priority within group	Vector (ID)	Description/Source	INT
	PDPINTB	1 (highest)	0019h	Power Drive Protection Interrupt B	1
A	CMP4INT	2	0024h	Compare Unit 4 compare interrupt	2
	CMP5INT	3	0025h	Compare Unit 5 compare interrupt	2
	CMP6INT	4	0026h	Compare Unit 6 compare interrupt	2
	T3PINT	5	002Fh	GP Timer 3 period interrupt	2
	T3CINT	6	0030h	GP Timer 3 compare interrupt	2
	T3UFINT	7	0031h	GP Timer 3 underflow interrupt	2
	T3OFINT	8 (lowest)	0032h	GP Timer 3 overflow interrupt	2
B	T4PINT	1 (highest)	0039h	GP Timer 4 period interrupt	3
	T4CINT	2	003Ah	GP Timer 4 compare interrupt	3
	T4UFINT	3	003Bh	GP Timer 4 underflow interrupt	3
	T4OFINT	4	003Ch	GP Timer 4 overflow interrupt	3
C	CAP4INT	1 (highest)	0036h	Capture Unit 4 interrupt	4
	CAP5INT	2	0037h	Capture Unit 5 interrupt	4
	CAP6INT	3	0038h	Capture Unit 6 interrupt	4

EVA Interrupt Flag Register A (EVAIFRA) — Address 742Fh

15-11	10	9	8
Reserved	T1OFINT FLAG	T1UFINT FLAG	T1CINT FLAG
R–0	RW1C–0	RW1C–0	RW1C–0

7	6-4	3	2	1	0
T1PINT FLAG	Reserved	CMP3INT FLAG	CMP2INT FLAG	CMP1INT FLAG	PDPINTA FLAG
RW1C–0	R–0	RW1C–0	RW1C–0	RW1C–0	RW1C–0

Note: *R = read access, W1C = write 1 to clear, -0 = value after reset.*

Bits 15–11 Reserved. Reads return zero; writes have no effect.

Bit 10 T1OFINT FLAG. GP Timer 1 overflow interrupt.

Read:	0	Flag is reset
	1	Flag is set
Write:	0	No effect
	1	Resets flag

Bit 9 T1UFINT FLAG. GP Timer 1 underflow interrupt.

Read:	0	Flag is reset
	1	Flag is set
Write:	0	No effect
	1	Resets flag

Bit 8 T1CINT FLAG. GP Timer 1 compare interrupt.

Read:	0	Flag is reset
	1	Flag is set
Write:	0	No effect
	1	Resets flag

Bit 7 T1PINT FLAG. GP Timer 1 period interrupt.

Read:	0	Flag is reset
	1	Flag is set
Write:	0	No effect
	1	Resets flag

Bits 6–4 Reserved. Reads return zero; writes have no effect.

Bit 3 CMP3INT FLAG. Compare 3 interrupt.

Read:	0	Flag is reset
	1	Flag is set
Write:	0	No effect
	1	Resets flag

Bit 2 **CMP2INT FLAG**. Compare 2 interrupt.
Read: 0 Flag is reset
1 Flag is set
Write: 0 No effect
1 Resets flag

Bit 1 **CMP1INT FLAG**. Compare 1 interrupt.
Read: 0 Flag is reset
1 Flag is set
Write: 0 No effect
1 Resets flag

Bit 0 **PDPINTA FLAG**. Power drive protection interrupt.
Read: 0 Flag is reset
1 Flag is set
Write: 0 No effect
1 Resets flag

EVA Interrupt Flag Register B (EVAIFRB) — Address 7430h

15-4	3	2	1	0
Reserved	T2OFINT FLAG	T2UFINT FLAG	T2CINT FLAG	T2PINT FLAG
R–0	RW1C–0	RW1C–0	RW1C–0	RW1C–0

Note: *R = read access, W1C = write 1 to clear, -0 = value after reset.*

Bits 15–4 **Reserved**. Reads return zero; writes have no effect.

Bit 3 **T2OFINT FLAG**. GP Timer 2 overflow interrupt.
Read: 0 Flag is reset
1 Flag is set
Write: 0 No effect
1 Resets flag

Bit 2 **T2UFINT FLAG**. GP Timer 2 underflow interrupt.
Read: 0 Flag is reset
1 Flag is set
Write: 0 No effect
1 Resets flag

Bit 1 **T2CINT FLAG**. GP Timer 2 compare interrupt.
Read: 0 Flag is reset
1 Flag is set
Write: 0 No effect
1 Resets flag

Bit 0 **T2PINT FLAG**. GP Timer 2 period interrupt.
Read: 0 Flag is reset
1 Flag is set
Write: 0 No effect
1 Resets flag

EVA Interrupt Flag Register C (EVAIFRC) — Address 7431h

15-3	2	1	0
Reserved	CAP3INT FLAG	CAP2INT FLAG	CAP1INT FLAG
R–0	RW1C–0	RW1C–0	RW1C–0

Note: *R = read access, W1C = write 1 to clear, -0 = value after reset.*

Bits 15–3 **Reserved**. Reads return zero; writes have no effect.

Bit 2 **CAP3INT FLAG**. Capture 3 interrupt.
Read: 0 Flag is reset
1 Flag is set
Write: 0 No effect
1 Resets flag

Bit 1 **CAP2INT FLAG**. Capture 2 interrupt.
Read: 0 Flag is reset
1 Flag is set
Write: 0 No effect
1 Resets flag

Bit 0 **CAP1INT FLAG**. Capture 1 interrupt.
Read: 0 Flag is reset
1 Flag is set
Write: 0 No effect
1 Resets flag

EVA Interrupt Mask Register A (EVAIMRA) — Address 742Ch

15-11	10	9	8
Reserved	T1OFINT ENABLE	T1UFINT ENABLE	T1CINT ENABLE
R–0	RW–0	RW–0	RW–0

7	6-4	3	2	1	0
T1PINT ENABLE	Reserved	CMP3INT ENABLE	CMP2INT ENABLE	CMP1INT ENABLE	PDPINTA ENABLE
RW–0	R–0	RW–0	RW–0	RW–0	RW–1

Note: *R = read access, W = write access, value following dash (–) = value after reset.*

Bits 15–11 Reserved. Reads return zero; writes have no effect.

Bit 10 T1OFINT ENABLE
0 Disable
1 Enable

Bit 9 T1UFINT ENABLE
0 Disable
1 Enable

Bit 8 T1CINT ENABLE
0 Disable
1 Enable

Bit 7 T1PINT ENABLE
0 Disable
1 Enable

Bits 6–4 Reserved. Reads return zero; writes have no effect.

Bit 3 CMP3INT ENABLE
0 Disable
1 Enable

Bit 2 CMP2INT ENABLE
0 Disable
1 Enable

Bit 1 CMP1INT ENABLE
0 Disable
1 Enable

Bit 0 PDPINTA ENABLE. This is enabled (set to 1) following reset.
0 Disable
1 Enable

EVA Interrupt Mask Register B (EVAIMRB) — Address 742Dh

15-4	3	2	1	0
Reserved	T2OFINT ENABLE	T2UFINT ENABLE	T2CINT ENABLE	T2PINT ENABLE
R–0	RW–0	RW–0	RW–0	RW–0

Note: *R = read access, W = write access, -0 = value after reset.*

Bits 15–4 Reserved. Reads return zero; writes have no effect.

Bit 3 T2OFINT ENABLE
0 Disable
1 Enable

Bit 2 T2UFINT ENABLE
0 Disable
1 Enable

Bit 1 T2CINT ENABLE
0 Disable
1 Enable

Bit 0 T2PINT ENABLE
0 Disable
1 Enable

EVA Interrupt Mask Register C (EVAIMRC) — Address 742Eh

15-3	2	1	0
Reserved	CAP3INT ENABLE	CAP2INT ENABLE	CAP1INT ENABLE
R–0	RW–0	RW–0	RW–0

Note: *R = read access, W = write access, -0 = value after reset.*
Bits 15–3 Reserved. Reads return zero; writes have no effect.

Bit 2 CAP3INT ENABLE
0 Disable
1 Enable

Bit 1 CAP2INT ENABLE
0 Disable
1 Enable

Bit 0 CAP1INT ENABLE
0 Disable
1 Enable

EVB Interrupt Flag Register A (EVBIFRA) — Address 752Fh

15-11	10	9	8
Reserved	T3OFINT FLAG	T3UFINT FLAG	T3CINT FLAG
R–0	RW1C–0	RW1C–0	RW1C–0

7	6-4	3	2	1	0
T3PINT FLAG	Reserved	CMP6INT FLAG	CMP5INT FLAG	CMP4INT FLAG	PDPINTB FLAG
RW1C–0	R–0	RW1C–0	RW1C–0	RW1C–0	RW1C–0

Note: *R = read access, W1C = write 1 to clear, -0 = value after reset.*

Bits 15–11 Reserved. Reads return zero; writes have no effect.

Bit 10 T3OFINT FLAG. GP Timer 3 overflow interrupt.

Read:	0	Flag is reset
	1	Flag is set
Write:	0	No effect
	1	Resets flag

Bit 9 T3UFINT FLAG. GP Timer 3 underflow interrupt.

Read:	0	Flag is reset
	1	Flag is set
Write:	0	No effect
	1	Resets flag

Bit 8 T3CINT FLAG. GP Timer 3 compare interrupt.

Read:	0	Flag is reset
	1	Flag is set
Write:	0	No effect
	1	Resets flag

Bit 7 T3PINT FLAG. GP Timer 3 period interrupt.

Read:	0	Flag is reset
	1	Flag is set
Write:	0	No effect
	1	Resets flag

Bits 6–4 Reserved. Reads return zero; writes have no effect.

Bit 3 CMP6INT FLAG. Compare 6 interrupt.

Read:	0	Flag is reset
	1	Flag is set
Write:	0	No effect
	1	Resets flag

Bit 2 CMP5INT FLAG. Compare 5 interrupt.

Read:	0	Flag is reset
	1	Flag is set
Write:	0	No effect
	1	Resets flag

Bit 1 CMP4INT FLAG. Compare 4 interrupt.

Read:	0	Flag is reset
	1	Flag is set
Write:	0	No effect
	1	Resets flag

Bit 0 **PDPINTB FLAG**. Power drive protection interrupt.
Read: 0 Flag is reset
1 Flag is set
Write: 0 No effect
1 Resets flag

EVB Interrupt Flag Register B (EVBIFRB) — Address 7530h

15-4	3	2	1	0
Reserved	T4OFINT FLAG	T4UFINT FLAG	T4CINT FLAG	T4PINT FLAG
R–0	RW1C–0	RW1C–0	RW1C–0	RW1C–0

Note: *R = read access, W1C = write 1 to clear, -0 = value after reset.*

Bits 15–4 **Reserved**. Reads return zero; writes have no effect.

Bit 3 **T4OFINT FLAG**. GP Timer 4 overflow interrupt.
Read: 0 Flag is reset
1 Flag is set
Write: 0 No effect
1 Resets flag

Bit 2 **T4UFINT FLAG**. GP Timer 4 underflow interrupt.
Read: 0 Flag is reset
1 Flag is set
Write: 0 No effect
1 Resets flag

Bit 1 **T4CINT FLAG**. GP Timer 4 compare interrupt.
Read: 0 Flag is reset
1 Flag is set
Write: 0 No effect
1 Resets flag

Bit 0 **T4PINT FLAG**. GP Timer 4 period interrupt.
Read: 0 Flag is reset
1 Flag is set
Write: 0 No effect
1 Resets flag

EVB Interrupt Flag Register C (EVBIFRC) — Address 7531h

15-3	2	1	0
Reserved	CAP6INT FLAG	CAP5INT FLAG	CAP4INT FLAG
R–0	RW1C–0	RW1C–0	RW1C–0

Note: *R = read access, W1C = write 1 to clear, -0 = value after reset.*

Bits 15–3 **Reserved**. Reads return zero; writes have no effect.

Bit 2 **CAP6INT FLAG**. Capture 6 interrupt.

Read:	0	Flag is reset
	1	Flag is set
Write:	0	No effect
	1	Resets flag

Bit 1 **CAP5INT FLAG**. Capture 5 interrupt.

Read:	0	Flag is reset
	1	Flag is set
Write:	0	No effect
	1	Resets flag

Bit 0 **CAP4INT FLAG**. Capture 4 interrupt.

Read:	0	Flag is reset
	1	Flag is set
Write:	0	No effect
	1	Resets flag

EVB Interrupt Mask Register A (EVBIMRA) — Address 752Ch

15-11	10	9	8
Reserved	T3OFINT ENABLE	T3UFINT ENABLE	T3CINT ENABLE
R–0	RW–0	RW–0	RW–0

7	6-4	3	2	1	0
T3PINT ENABLE	Reserved	CMP6INT ENABLE	CMP5INT ENABLE	CMP4INT ENABLE	PDPINTB ENABLE
RW–0	R–0	RW–0	RW–0	RW–0	RW–1

Note: *R = read access, W = write access, -n = value after reset.*

Bits 15–11 **Reserved**. Reads return zero; writes have no effect.

Bit 10 T3OFINT ENABLE
0 Disable
1 Enable

Bit 9 T3UFINT ENABLE
0 Disable
1 Enable

Bit 8 T3CINT ENABLE
0 Disable
1 Enable

Bit 7 T3PINT ENABLE
0 Disable
1 Enable

Bits 6–4 Reserved. Reads return zero; writes have no effect.

Bit 3 CMP6INT ENABLE
0 Disable
1 Enable

Bit 2 CMP5INT ENABLE
0 Disable
1 Enable

Bit 1 CMP4INT ENABLE
0 Disable
1 Enable

Bit 0 PDPINTB ENABLE. This is enabled (set to 1) following reset.
0 Disable
1 Enable

EVB Interrupt Mask Register B (EVBIMRB) — Address 752Dh

15-4	3	2	1	0
Reserved	T4OFINT ENABLE	T4UFINT ENABLE	T4CINT ENABLE	T4PINT ENABLE
R–0	RW–0	RW–0	RW–0	RW–0

Note: *R = read access, W = write access, -0 = value after reset.*

Bits 15–4 Reserved. Reads return zero; writes have no effect.

Bit 3 T4OFINT ENABLE
0 Disable
1 Enable

Bit 2 T4UFINT ENABLE
0 Disable
1 Enable

Bit 1 T4CINT ENABLE
0 Disable
1 Enable

Bit 0 T4PINT ENABLE
0 Disable
1 Enable

EVB Interrupt Mask Register C (EVBIMRC) — Address 752Eh

15-3	2	1	0
Reserved	CAP6INT ENABLE	CAP5INT ENABLE	CAP4INT ENABLE
R–0	RW–0	RW–0	RW–0

Note: *R = read access, W = write access, -0 = value after reset.*

Bits 15–3 Reserved. Reads return zero; writes have no effect.

Bit 2 CAP6INT ENABLE
0 Disable
1 Enable

Bit 1 CAP5INT ENABLE
0 Disable
1 Enable

Bit 0 CAP4INT ENABLE
0 Disable
1 Enable

6.3 General Purpose (GP) Timers

A General Purpose (GP) timer is simply a 16-bit counter, which may be configured to count up, down, or continuously up and down. There are two GP Timers in each EV: Timer1 and Timer2 for EVA and Timer3 and Timer4 for EVB.

All timers use the CPU clock as a general timing reference, but each individual timer may use a "pre-scaled" or frequency reduced time base which is specified in each timer's control register.

A GP Timer may also be configured to generate an interrupt or trigger another peripheral on certain events such as a timer overflow (timer reached period value), underflow (timer reached zero), or compare (timer value reached compare value). Some examples of uses for the GP Timers include: setting the sampling period for the ADC by triggering the start of conversion; or providing the switching period for the generation of a PWM signal.

Figure 6.3 shows a block diagram of a GP Timer. There are two cases that apply to Fig. 6.3:

1. When "x" = 2, "y" = 1 and "n" = 2
2. When "x" = 4, "y" = 3 and "n" = 4

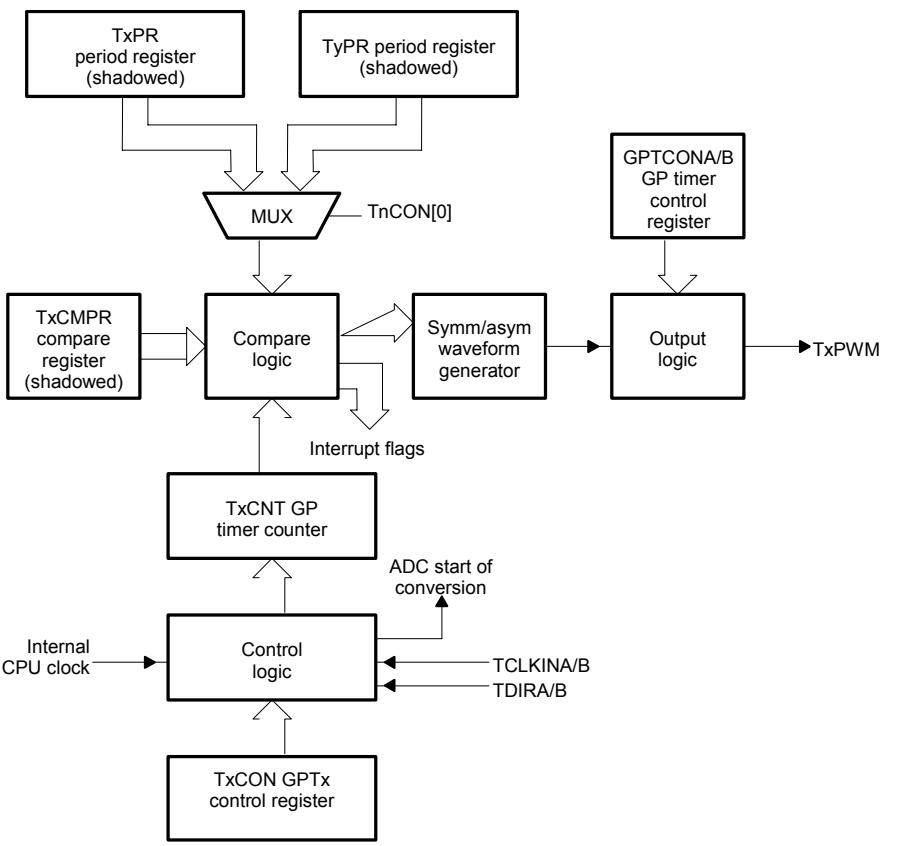

Figure 6.3 General purpose timer configuration diagram.

Each GP Timer consists of the following components:

- One readable and writeable (RW) 16-bit up and up/down counter register **TxCNT** (x = 1, 2, 3, 4). This register holds the current count value and increments or decrements depending on the direction of counting
- 16-bit timer compare register, **TxCMPR** (x = 1, 2, 3, 4)
- 16-bit timer period register, **TxPR** (x = 1, 2, 3, 4)
- 16-bit individual timer control register, **TxCON** (x = 1, 2, 3, 4)
- Programmable input clock divider (pre-scaler) applicable to both internal and external clock inputs
- One GP Timer compare output pin, **TxCMP** (x = 1, 2, 3, 4)
- Interrupt logic

6.3.1 GP Timer Inputs and Outputs

Each GP Timer has the following inputs:

- Clock Reference Inputs: (1) The internal device (CPU) clock and (2) external clock, TCLKINA/B, that has a maximum frequency of one-fourth that of the device clock
- Direction input, TDIRA/B, when a GP Timer is in directional up/down-counting mode
- Reset signal, RESET

The source of the GP Timer clock can be the internal CPU clock signal or the external clock input, TCLKINA/B. The frequency of the external clock must be less than or equal to one-fourth of that of the device clock. GP Timer 2 (EVA) and GP Timer 4 (EVB) can be used with the QEP circuits in directional up-/down-counting mode. In this case, the QEP circuits provide both the clock and direction inputs to the timer. A wide range of prescale factors are provided for the clock input to each GP Timer.

The QEP circuit, when selected, can generate the input clock and counting direction for GP Timer 2/4 in the directional up-/down-counting mode. A QEP signal may come from a rotary encoder which is attached to a motor shaft to provide speed/direction feedback. Via the QEP circuitry, it controls the clock input and direction of Timer 2/4. From this, the speed of the motor can be determined from the counting speed; the direction of count reflects the rotation direction. The QEP input clock cannot be scaled by GP Timer prescaler circuits (the prescaler of the selected GP Timer has no effect if the QEP circuit is selected as the clock source). Furthermore, the frequency of the clock generated by the QEP circuits is four times that of the frequency of each QEP input channel because the rising and falling edges of both QEP input channels are counted by the selected timer. In other words, the frequency of the incoming QEP signal must be less than or equal to one-fourth of that of the CPU clock.

Now that the inputs to the GP Timers have been discussed, we will next discuss the outputs associated with each GP Timer. Outputs are either connected to a data

memory mapped register, another peripheral, or an external pin of the LF2407. Each GP Timer has the following outputs:

- GP Timer compare outputs TxCMP, x = 1, 2, 3, 4 (external pins on the LF2407)
- ADC start-of-conversion signal (connected to the ADC module)
- Underflow, overflow, compare match, and period match signals to its own compare logic and to the compare units (connected to the compare units of the EV)
- Counting direction indication bits (in the GPTCONA/B registers mapped to data memory)

The General Purpose Timer Control Register (GPTCONA/B), configures the action to be taken by the timers on different timer events, and indicates the counting directions of the GP Timers. GPTCONA/B is readable and writeable, although writing to the status bits in this register has no effect.

6.3.2 GP Counting Operation

GP Timers have four possible modes of counting operation:

1. Stop/Hold mode
2. Continuous Up-Counting mode
3. Directional Up/Down-Counting mode
4. Continuous Up/Down-Counting mode

Each timer is configured for desired counting mode in its corresponding Timer Control register (TxCON). Each GP Timer is enabled by setting the Timer Enable bit each timer's control register. When the timer is enabled, the timer counts according to the counting mode specified by the bits in the TxCON. The counting direction of the GP Timers are reflected by their respective bit in GPTCONA/B. When the timer is disabled (enable bit=0), counting is disabled and the prescaler of that timer is reset to the default value of "x/1".

Stop/Hold mode is like the "pause" button for the timer. In stop/hold mode the GP Timer stops and holds at its current state. The timer counter, the compare output, and the pre-scale select all remain unchanged.

Continuous Up-Counting Mode:

The continuous up-counting mode is useful in creating asymmetric PWM signals. In the continuous up-count mode the following events occur:

1. The GP Timer in this mode counts up in sync with the pre-scaled input clock until the value of the timer counter matches that of the period register.
2. On the next rising edge of the input clock after the match, the GP Timer resets to zero and starts counting up again.
3. The period interrupt flag of the timer is set one clock cycle after the match between the timer counter and period register. If the flag is not masked, a

peripheral interrupt request is generated. An ADC start is sent to the ADC module at the same time the flag is set if the period interrupt of this timer has been selected by the appropriate bits in GPTCONA/B to start the ADC.

4. One clock cycle after the GP Timer becomes 00001, the underflow interrupt flag of the timer is set. A peripheral interrupt request is generated by the flag if it is unmasked. An ADC start is sent to the ADC module at the same time if the underflow interrupt flag of this timer has been selected by the appropriate bits in the GPTCONA/B to start the ADC.

The duration of the timer period is (TxPR) + 1 cycles of the scaled clock input except for the first period. The duration of the first period is the same if the timer counter is zero when counting starts. The initial value of the GP Timer can be any value from 0h to FFFFh. When the initial value is greater than the value in the period register, the timer counts up to FFFFh, resets to zero, and continues the operation as if the initial value was zero. The overflow interrupt flag is set one clock cycle after the value in TxCNT matches FFFFh. A peripheral interrupt request is generated by the flag if it is unmasked.

When the initial value in the timer counter is the same as that of the period register, the timer sets the period interrupt flag, resets to zero, sets the underflow interrupt flag, and then continues the operation again as if the initial value was zero. If the initial value of the timer is between zero and the contents of the period register, the timer counts up to the period value and continues to finish the period as if the initial counter value was the same as that of the period register.

The counting direction indication bit in GPTCONA/B is "1" for the timer in this mode. Either the external or internal device clock can be selected as the input clock to the timer. The TDIRA/B input is ignored by the GP Timer in this mode since we are in an up-count only mode. The continuous up-count mode of the GP Timer is particularly useful for the generation of edge-triggered or asynchronous PWM waveforms and sampling periods in many motor and motion control systems. Figure 6.4 shows the continuous up-counting mode of the GP Timer.

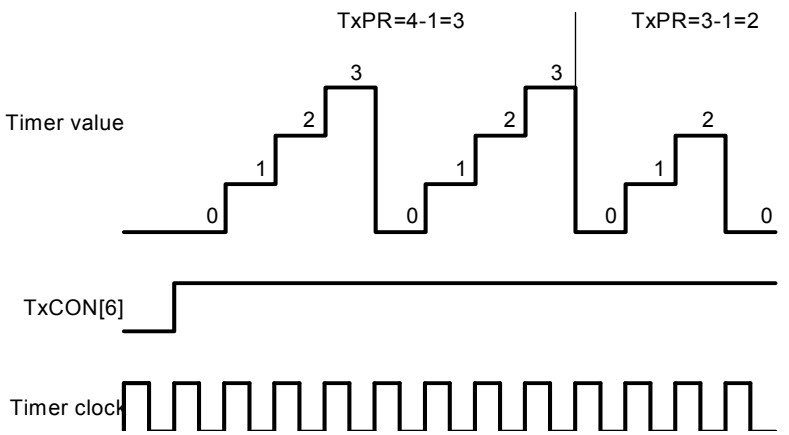

Figure 6.4 Operation of continuous up-counting mode (TxPR = 3 or 2).

Directional Up/Down-Counting Mode:

A GP Timer in directional up/down-counting mode counts either up or down according to the pre-scaled clock and TDIRA/B inputs. The input pin TDIRA/B determines the direction of counting when the GP Timer is in directional up/down-counting mode. When TDIRA/B is high, upward counting is specified; when TDIRA/B is low, downward counting is specified.

When the TDIRA/B pin is held high, the GP Timer will count up until it reaches the value of the period register. When the timer value equals that of its period register the timer will reset to zero and start counting up to the period again. The initial value of the timer can be any value between 0000h to FFFFh. In the case that the initial value of the timer counter is greater than that of the period register, the timer would count up to FFFFh before resetting itself to zero and continuing the counting operation. When TDIRA/B pin is held low, the GP Timer will count down from whatever initial value the counter was at until its count value becomes zero. When its count value becomes zero, the value of the period register is automatically loaded into the count value register and the timer begins counting down to zero.

In the directional up/down mode, the period, underflow, and overflow interrupt flags, interrupts, and associated actions are generated on respective events in the same manner as they are generated in the continuous up-counting mode. The direction of counting is indicated for the timer in this mode by the corresponding direction indication bit in GPTCONA/B: 1 means counting up; 0 means counting down. Either the external clock from the TCLKINA/B pin or the internal device clock can be used as the input clock for the timer in this mode. Figure 6.5 shows the directional up-/down-counting mode of the GP Timers.

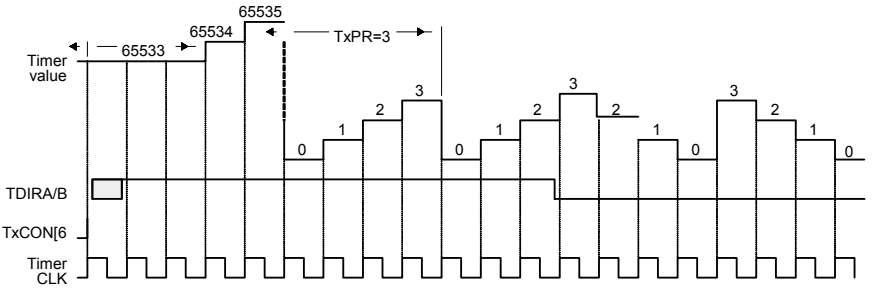

Figure 6.5 GP timer directional up/down-counting mode: prescale factor 1 and TxPR = 3A.

Additionally, the directional up-/down-counting mode of GP Timer 2 and 4 can also be used with the Quadrature Encoder Pulse (QEP) circuits in the EV module. While the QEP circuits are active, they provide both the counting clock and direction for GP Timers 2 or 4.

Continuous Up/Down-Counting Mode

The continuous up/down-counting mode is useful in generating symmetric PWM waveforms. This mode of operation is the same as the directional up-/down-counting mode, except for the fact that the TDIRA/B pin has no effect on the counting direction. The counting direction changes from up to down when the timer reaches the period value. The timer direction changes from down to up when the timer reaches zero. Continuous up/down-counting mode is particularly useful in generating centered or symmetric PWM waveforms.

The initial value of the GP Timer counter can be any value from 0h to FFFFh. When the initial value is greater than that of the period register (TxPR), the timer counts up to FFFFh, resets to zero, and continues the operation as if the initial value were zero. If the initial value of the timer counter is the same as that of the period register, the timer counts down to zero and continues again as if the initial value were zero. If the initial value of the timer is between zero and the contents of the period register, the timer will count up to the period value and continue to finish the period as if the initial counter value were the same as that of the period register.

The counting direction indication bit in the GPTCONA/B indicates "1" when the timer counts upward and "0" when the timer is counting downward. Either an external clock reference from the TCLKINA/B pin or the internal CPU clock can be selected as the input clock. Since the change of count direction is automatic in this mode, the TDIRA/B pin has no effect. The period, underflow, and overflow interrupt flags, interrupts, and associated actions are generated on the respective events in the same manner as they are generated in other counting modes. Figure 6.6 shows the continuous up-/down-counting mode of the GP Timer.

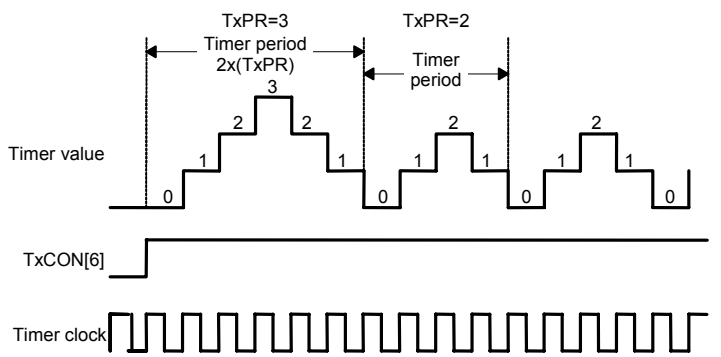

Figure 6.6 Continuous up/down counting mode (timer period register = 3 or 2).

Note: *The period of the timer in this mode is 2*(TxPR) cycles of the scaled clock input, except for the first period.*

6.3.3 Control Registers Associated with the General Purpose Timers

Individual Timer Control Registers (TxCON), where x=1,2,3,4

The operational mode of each GP Timer is controlled by the timer's corresponding control register (TxCON). The bits in the TxCON configure:

1. What counting mode the timer is set for
2. Whether the internal (CPU) or an external clock is to be used for the clock reference
3. Which of the eight input clock pre-scale factors (ranging from 1/1 to 1/128) is used
4. When (on which condition) the timer compare register is reloaded
5. Whether the timer is enabled or disabled
6. Whether the timer compare operation is enabled or disabled
7. Which period register is used by timer 2 (its own, or timer 1's period register (EVA))
8. Which period register is used by timer 4 (its own, or timer 3's period register (EVB))

In EVA, GP Timer 2 can be synchronized with GP Timer 1. Additionally, in EVB, GP Timer 4 can be synchronized with GP Timer 3 by configuring T2CON and T4CON, respectively, in the following ways:

EVA:

1. Set the T2SWT1 bit in T2CON to start GP Timer 2 counting with the TENABLE bit in T1CON (both timer counters start simultaneously)
2. Initialize the timer counter in GP Timers 1 and 2 with different values before starting synchronized operation
3. Specify that GP Timer 2 uses the period register of GP Timer 1 as its period register (ignoring its own period register) by setting SELT1PR in T2CON

EVB:

1. Set the T4SWT3 bit in T4CON to start GP Timer 4 counting with the TENABLE bit in T3CON (thus, both timer counters start simultaneously)
2. Initialize the timer counters in GP Timers 3 and 4 with different values before starting synchronized operation
3. Specify that GP Timer 4 uses the period register of GP Timer 3 as its period register (ignoring its own period register) by setting SELT3PR in T4CON

This allows the desired synchronization between GP Timer events. Since each GP Timer starts the counting operation from its current value in the counter register, one GP Timer can be programmed to start with a known delay after the other GP Timer.

Timer x Control Register Bit Descriptions (TxCON; x = 1, 2, 3, or 4) — Addresses: 7404h (T1CON), 7408h (T2CON), 7504h (T3CON), and 7508h (T4CON)

15	14	13	12	11	10	9	8
Free	Soft	Reserved	TMODE1	TMODE0	TPS2	TPS1	TPS0
RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0
7	6	5	4	3	2	1	0
T2SWT1/ T4SWT3†	TENABLE	TCLKS1	TCLKS0	TCLD1	TCLD0	TECMPR	SELT1PR/ SELT3PR†
RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

† Reserved in T1CON andT3CON

Note: *R = read access, W = write access, -0 = value after reset.*

Bits 15–14 Free, Soft. Emulation control bits.

00 Stop immediately on emulation suspend
01 Stop after current timer period is complete on emulation suspend
10 Operation is not affected by emulation suspend
11 Operation is not affected by emulation suspend

Bit 13 Reserved. Reads return zero, writes have no effect.

Bits 12–11 TMODE1–TMODE0. Count Mode Selection.

00 Stop/Hold
01 Continuous-Up/-Down Count Mode
10 Continuous-Up Count Mode
11 Directional-Up/-Down Count Mode

Bits 10–8 TPS2–TPS0.

Input Clock Prescaler.
000=x/1 , 001=x/2, 010=x/4, 011=x/8, 100=x/16, 101=x/32,110=x/64
111=x/128 ; x = device (CPU) clock frequency

Bit 7 T2SWT1. In the case of EVA, this bit is T2SWT1. (GP Timer 2 start with GP Timer 1.) Start GP Timer 2 with GP Timer 1's timer enable bit. This bit is reserved in T1CON.
T4SWT3. In the case of EVB, this bit is T4SWT3. (GP Timer 4 start with GP Timer 3.) Start GP Timer 4 with GP Timer 3's timer enable bit. This bit is reserved in T3CON.

0 Use own TENABLE bit
1 Use TENABLE bit of T1CON (in case of EVA) or T3CON (in case of EVB) to enable and disable operation ignoring own TENABLE bit

Bit 6 **TENABLE**. Timer enable.

0	Disable timer operation (the timer is put in hold and the prescaler counter is reset)
1	Enable timer operations

Bits 5–4 TCLKS1, TCLKS0. Clock Source Select.

5	4	Source
0	0	Internal
0	1	External
1	0	Reserved
1	1	QEP Circuit† (in case of Timer 2/Timer 4) Reserved (in case of Timer 1/Timer 3)
†		This option is valid only if SELT1PR = 0

Bits 3–2 TCLD1, TCLD0. Timer Compare Register Reload Condition.

00	When counter is 0
01	When counter value is 0 or equals period register value
10	Immediately
11	Reserved

Bit 1 **TECMPR**. Timer compare enable.

0	Disable timer compare operation
1	Enable timer compare operation

Bit 0 **SELT1PR**. In the case of EVA, this bit is SELT1PR (Period register select).

When set to 1 in T2CON, the period register of Timer 1 is chosen for Timer 2 also, ignoring the period register of Timer 2. This bit is a reserved bit in T1CON. **SELT3PR**. In the case of EVB, this bit is SELT3PR (Period register select). When set to 1 in T4CON, the period register of Timer 3 is chosen for Timer 4 also, ignoring the period register of Timer 4. This bit is a reserved bit in T3CON.

0	Use own period register
1	Use T1PR (in case of EVA) or T3PR (in case of EVB) as period register ignoring own period register

Overall GP Timer Control Registers (GPTCONA/B)

The control register GPTCONA/B specifies the action to be taken by the timers on different timer events. This register also has timer direction status bits that display the current direction of the timers. Also, the polarity of the GP Timer compare outputs is configured here. Bits in GPTCONA/B can also configure specific timers to trigger an ADC start signal when an underflow, compare match, or period match occurs. This feature requires that the ADC also be configured to

accept the start of conversion signal from the GP Timer. Having the GP Timer trigger provides for automatic synchronization between the GP Timer event and the ADC.

GP Timer Control Register A (GPTCONA) Bit Descriptions — Address 7400h

15	14	13	12-11	10-9	8-7
Reserved	T2STAT	T1STAT	Reserved	T2TOADC	T1TOADC
RW–0	R–1	R–1	RW–0	RW–0	RW–0

6	5-4	3-2	1-0
TCOMPOE	Reserved	T2PIN	T1PIN
RW–0	RW–0	RW–0	RW–0

Note: *R = read access, W = write access, -n = value after reset.*

Bit 15 **Reserved**. Reads return zero; writes have no effect.

Bit 14 **T2STAT**. GP Timer 2 Status. Read only.
- 0 Counting downward
- 1 Counting upward

Bit 13 **T1STAT**. GP Timer 1 Status. Read only.
- 0 Counting downward
- 1 Counting upward

Bits 12–11 Reserved. Reads return zero; writes have no effect.

Bits 10–9 T2TOADC. Start ADC with timer 2 event.
- 00 No event starts ADC
- 01 Setting of underflow interrupt flag starts ADC
- 10 Setting of period interrupt flag starts ADC
- 11 Setting of compare interrupt flag starts ADC

Bits 8–7 T1TOADC. Start ADC with timer 1 event.
- 00 No event starts ADC
- 01 Setting of underflow interrupt flag starts ADC
- 10 Setting of period interrupt flag starts ADC
- 11 Setting of compare interrupt flag starts ADC

Bit 6 **TCOMPOE**. Compare output enable. If PDPINTx is active this bit is set to zero.
- 0 Disable all GP Timer compare outputs (all compare outputs are put in the high-impedance state)
- 1 Enable all GP Timer compare outputs

Bits 5–4 Reserved. Reads return zero; writes have no effect.

Bits 3–2 T2PIN. Polarity of GP Timer 2 compare output.
- 00 Forced low
- 01 Active low
- 10 Active high
- 11 Forced high

Bits 1–0 T1PIN. Polarity of GP Timer 1 compare output.
- 00 Forced low
- 01 Active low
- 10 Active high
- 11 Forced high

GP Timer Control Register B (GPTCONB) Bit Descriptions — Address 7500h

15	14	13	12-11	10-9	8-7
Reserved	T4STAT	T3STAT	Reserved	T4TOADC	T3TOADC
RW–0	R–1	R–1	RW–0	RW–0	RW–0

6	5-4	3-2	1-0
TCOMPOE	Reserved	T4PIN	T3PIN
RW–0	RW–0	RW–0	RW–0

Note: *R = read access, W = write access, -n = value after reset.*

Bit 15 Reserved. Reads return zero; writes have no effect.

Bit 14 T4STAT. GP Timer 4 Status. Read only.
- 0 Counting downward
- 1 Counting upward

Bit 13 T3STAT. GP Timer 3 Status. Read only.
- 0 Counting downward
- 1 Counting upward

Bits 12–11 Reserved. Reads return zero; writes have no effect.

Bits 10–9 T4TOADC. Start ADC with timer 4 event.
- 00 No event starts ADC
- 01 Setting of underflow interrupt flag starts ADC
- 10 Setting of period interrupt flag starts ADC
- 11 Setting of compare interrupt flag starts ADC

Bits 8–7 T3TOADC. Start ADC with timer 3 event.
- 00 No event starts ADC
- 01 Setting of underflow interrupt flag starts ADC

10 Setting of period interrupt flag starts ADC
11 Setting of compare interrupt flag starts ADC

Bit 6 TCOMPOE. Compare output enable. If PDPINTx is active this bit is set to zero.
0 Disable all GP Timer compare outputs (all compare outputs are put in the high-impedance state)
1 Enable all GP Timer compare outputs

Bits 5–4 Reserved. Reads return zero; writes have no effect.

Bits 3–2 T4PIN. Polarity of GP Timer 4 compare output.
00 Forced low
01 Active low
10 Active high
11 Forced high

Bits 1–0 T3PIN. Polarity of GP Timer 3 compare output.
00 Forced low
01 Active low
10 Active high
11 Forced high

GP Timer Compare Registers (TxCMPR), x=1,2,3,4 – User Specified Value

Addresses 7402h (T1CMPR), 7406h (T2CMPR), 7502h (T3CMPR), 7506h (T4CMPR)

The compare register associated with each GP Timer stores the value that will be constantly compared with the current value of the GP Timer. When a compare match occurs, the following events also occur:

1. A transition occurs on the associated compare output according to the bit pattern in GPTCONA/B
2. The corresponding interrupt flag is set
3. A peripheral interrupt request is generated if the interrupt is unmasked
4. The compare operation of a GP Timer can be enabled or disabled by the appropriate bit in TxCON
5. The compare operation and outputs can be enabled in any of the timer counting modes, including the QEP circuit

GP Timer Period Registers (TxPR) – User Specified Value

Addresses 7403h (T1PR), 7407h (T2PR), 7503h (T3PR), 7507h (T4PR)

The period register determines the rate at which the timer resets itself or changes direction (the period of the timer). This register in combination with the input clock frequency (and clock pre-scale factor) determines the frequency of a

PWM signal created by the compare output pin. The corresponding timer either resets to "0", or starts counting downward (depending on the operating mode) when a match occurs between the period register and the timer counter (TxCNT).

CAUTION: *The period register of a GP Timer needs to be initialized before its counter is set to a non-zero value. Otherwise, the value of the period register will remain unchanged until the next underflow!*

Both the compare and period registers of the GP Timers are shadowed or double-buffered. This means that when either the period registers or compare registers are written to, the value is automatically stored first into a buffer register and then automatically written to the real register. The reason for this is to prevent the unacceptable situation such as a timer period register being written to and read from at the same time. Because of the register shadowing, a new value can be written to any of these registers at any time. The double buffering feature of the period and compare registers allows the user program to update the period and compare registers at any time in order to change the future timer period. Register shadowing is virtually transparent to the user. However, when configuring a compare unit, it is necessary to specify on what condition the actual compare register is reloaded from the buffer register. For the compare register, the content in the buffer register is loaded into the working (active) register **only** when the certain timer event specified by TxCON occurs. A compare register would be reloaded automatically either immediately after the shadow register is written, on underflow (GP Timer counter value equals "0"), on an underflow, or on period register match. In the case that the associated compare operation is disabled, any value written to the compare register is immediately loaded into the active register. The period register will be reloaded with the value in its buffer register only when the value of the counter register (TxCNT) becomes equal to "0". Except for the compare register reload condition, the user need not worry about register shadowing on the LF2407.

6.3.4 GP Timer Interrupts

There are 16 combined interrupt flags in the EVAIFRA, EVAIFRB, EVBIFRA, and EVBIFRB registers for the GP Timers. Each of the four GP Timers has the capability to generate up to four interrupts on the events listed in Table 6.3.

Table 6.3 General purpose timer interrupts

Interrupt Event	Interrupt Name (x=1,2,3,4)	Condition For Generation
Underflow	TxUFINT	When the counter reaches 0000h
Overflow	TxOFINT	When the counter reaches FFFFh
Compare Match	TxCINT	When the counter register contents match that of the compare register
Period Match	TxPINT	When the counter register contents match that of the period register

A timer compare "event" or match happens when the current count value of a GP Timer counter equals the value of the timer's compare register. The corresponding compare interrupt flag is set one clock cycle after the match if the compare operation is enabled. An overflow event occurs when the value of the timer counter reaches FFFFh. An underflow event occurs when the timer counter reaches 0000h. Similarly, a period event happens when the value of the timer counter is the same as that of the period register. The overflow, underflow, and period interrupt flags of the timer are set one clock cycle after the occurrence of each individual event. Note that these definitions of overflow and underflow are different from the conventional definitions the reader might be used to.

6.3.5 PWM Output and General Purpose Timer Compare Operation

A PWM waveform is a sequence of pulses with fixed frequency but varying pulse widths. The width of the pulse might vary from 0% to 100% of the fixed period. The pulse widths are modulated by another signal called the modulation signal. In order to generate a PWM signal digitally, a timer is set to continuously repeat a counting period. This period is known as the PWM carrier period. The inverse of the carrier period is called the carrier frequency.

The counting pattern of the timer will either be a "saw-tooth" (asymmetric) or "triangle" (symmetric) wave depending on what counting mode the timer has been configured for. As always, the compare value is constantly being compared with the value of the timer counter. When a match occurs, the output toggles High to Low, or Low to High. When the timer period value is reached or a second match occurs, the output toggles again. The on and off time of the pulse is directly dependent on the value loaded into the timer's compare register. By varying the number in the compare register by the modulation signal (usually a sinusoid), a PWM signal that represents the modulating signal can be produced.

The "output" discussed above refers to each GP Timer's associated PWM output pin (TxPWM). The logic level of the PWM output pin is determined automatically by hardware. This level is based on the value of the associated compare register and timer count value (see Fig. 6.7, note the compare match points and the output change at these points). If the compare operation is enabled in TxCON, the following events occur on a compare match:

1. The compare interrupt flag of the timer is set one clock cycle after the match.
2. A transition occurs on the associated PWM output pin one device clock cycle after the match according to the bit configuration in GPTCONA/B.
3. If the compare interrupt flag has been selected by the appropriate GPTCONA/B bits to start the ADC, an ADC start signal is generated at the same time the compare interrupt flag is set.
4. A peripheral interrupt request is generated by the compare interrupt flag if it is unmasked.

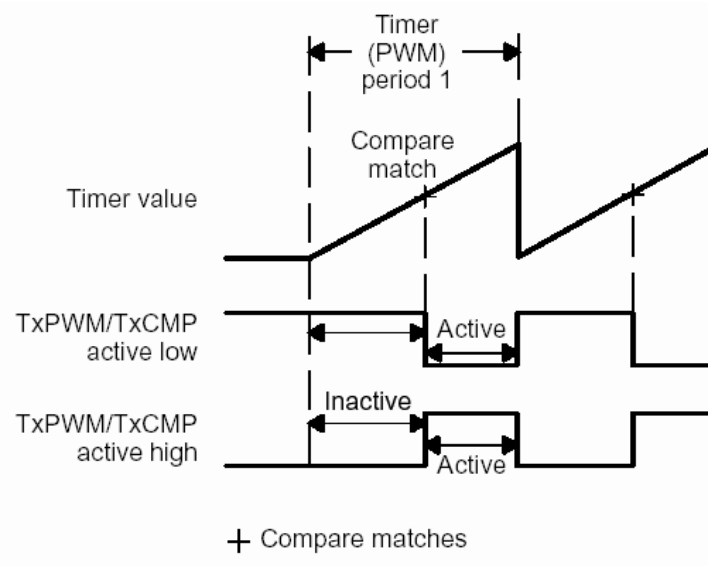

Figure 6.7 Timer compare match and associated change on TxPWM pin.

The polarity of the compare output (see diagram in Fig. 6.6) of a GP Timer can be specified active high, active low, forced high, or forced low. This polarity is determined by setting the bits in the GPTCONA/B register. If active low, the output changes from high to low on the first compare match. It then goes from low to high on the second compare match if the GP Timer is in an up/down-counting mode, or on period match if the GP Timer is in up-counting mode. If active high, the output changes from low to high on the first compare match. It then goes from high to low on the second compare match if the GP Timer is in an up-/down counting mode, or on period match if the GP Timer is in up-count mode. If forced low, the timer compare output becomes low immediately when it is specified. If forced high, the timer compare output becomes high immediately when it is specified.

By default (after a reset or power-on) all GP Timer PWM output pins are put in a high-impedance (HI-Z) state. The PWM output must be made active by configuring the GPTCONA/B registers. At anytime the PWM outputs will be made HI-Z whenever the power drive protection pin $\overline{PDPINTx}$ is active and is pulled low. Additionally, the corresponding PWM pin will be made HI-Z when bit 1 of the TxCON register is zeroed by software.

The transition on the PWM output pin is controlled by the asymmetric or symmetric timer waveform and the associated output logic. For an asymmetric wave form, the timer is set up in continuous up-count mode. To generate a symmetric waveform, the timer needs to be configured to continuous up/down counting.

Example 6.1 - Generation of an Asymmetric Waveform: The asymmetric waveform in Fig. 6.8 is generated when the GP Timer is in continuous up-counting mode. When in this mode the output changes in the following:

1. Output pin at "inactive level" before the counting operation starts
2. Output pin remains at "inactive level" until the compare match happens
3. Output toggles to "active level" on the compare match
4. Output remains unchanged at "active level" until the end of the period
5. At end of period, output resets to "inactive level"; that is if the new compare value is not zero

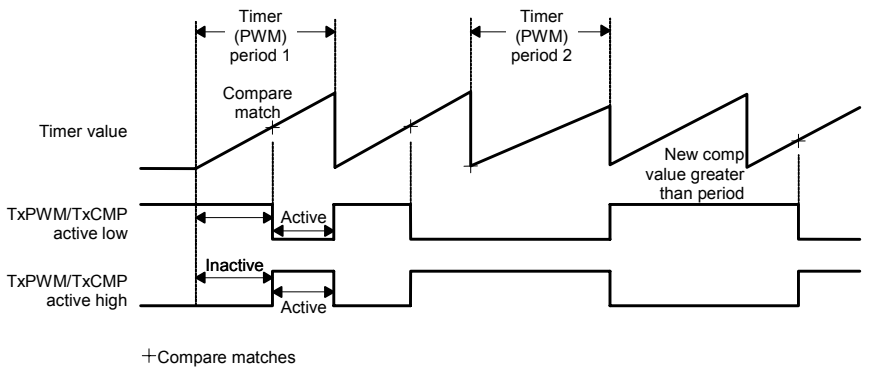

Figure 6.8 Asymmetric timer waveform generated by a GP timer in continuous up-count mode.

If the compare value is zero at the very beginning of the period, then a compare match is made at the very beginning and, consequently, the output is the active level for the period. If the output is "active" for the whole period and the new compare value for the next period is zero, then the output will stay at the active level so as not to cause a glitch. If the value in the compare register is greater than the value in the period register, then a compare match will never be made and consequently the output will be at the inactive level through the whole period.

The above allows the duty cycle of the PWM to range from 0 to 100% without glitches being present. If the compare value is the same as the period value, which causes a compare match, then the output pin will be at the active level for exactly one pre-scaled clock cycle.

Example 6.2 - Symmetric Waveform Generation: When the GP Timer is configured in continuous up/down-counting mode, a symmetric waveform is generated as in Fig. 6.9. The output changes in the following sequence:

1. "inactive level" before the counting operation starts
2. remains at "inactive level" until the compare match
3. toggles to "active level" on the first compare match

4. remains unchanged at "active level" until the second compare match
5. toggles to "inactive level" on the second compare match
6. remains unchanged at "inactive level" until the end of the period and remains unchanged until next compare match

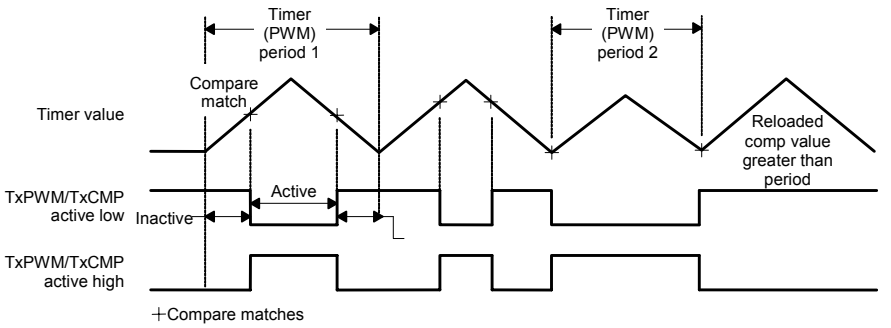

Figure 6.9 Symmetric timer waveform from continuous up/down count mode.

If the compare value is zero at the beginning of the period, the output is set to the active level at the beginning of a period and remains unchanged until the second compare match. After the first transition, the output remains at the active level until the end of the period if the compare value becomes zero for the second half of the period. When this happens, the output does not reset to zero if the new compare value for the following period is still zero.

This is done again to assure the generation of PWM pulses of 0% to 100% duty cycle without any glitches. The first transition does not happen if the compare value is greater than or equal to that of the period register for the first half of the period. However, the output still toggles when a compare match happens in the second half of the period. This error in output transition, often as a result of calculation error in the application routine, is corrected at the end of the period because the output resets to zero, unless the new compare value for the following period is zero. In this case, the output remains one, which again puts the output of the waveform generator in the correct state.

Calculations for Active and Inactive Time Periods

In order to utilize the GP Timer PWM outputs, it is sometimes necessary to calculate the active and inactive pulse times for the PWM output pins. We can find the active and inactive times for both the asymmetrical (Continuous Up-Count Mode) and symmetrical (Continuous Up/Down Count Mode). The calculation criteria for these times are as follows:

Continuous Up-Count Mode:

Active Output Pulse Time = [(TxPR) – (TxCMPR) + 1] cycles of the scaled input clock.

Inactive Output Pulse Time = (period of the scaled input clock) * (value of TxCMPR)

- When the value in TxCMPR is zero, the GP Timer compare output is active for the whole period.
- When TxCMPR is ≥ TxPR, the length of the active phase (the output pulse width) is zero.

Continuous Up/Down Counting Mode:

For the continuous up-/down-counting mode, the compare register can have different values while counting down and while counting up.

Active Output Pulse Time = [(TxPR) – (TxCMPR)**up** + (TxPR) – (TxCMPR)**dn**]** cycles of the scaled input clock

- If (TxCMPR) **up** is zero, the compare output is active at the beginning of the period. If (TxCMPR)dn is also zero, then output remains active until the end of the period.
- When (TxCMPR)**up** is ≥ (TxPR), the first transition is lost. Similarly, the second transition is lost when (TxCMPR)**dn** is ≥ (TxPR).
- If both (TxCMPR)up and TxCMPR)dn are greater than or equal to (TxPR), then the GP Timer compare output is inactive for the entire period.

**where (TxCMPR)up is the compare value on the timer's way up and (TxCMPR)dn is the compare value on the way down.

GP Timer PWM Generation -Practical Steps

To generate a PWM output signal on the GP Timer PWM outputs, make sure the following are configured to allow for PWM generation (also see Example 6.3):

1. Note what the PLL module is set to. The PLL provides the clock signal to the DSP and hence to the EV. In the timer control registers we have the option of pre-scaling (dividing) the clock signal to choose a time base for the GP Timers.
2. The corresponding EV pins need to be configured for their primary function in the appropriate MCRx register.
3. Initialize TxCNT (we usually set the count vale to zero)
4. Set TxPR according to the desired PWM (carrier) period. The TxPR value is calculated by the following formulas:

Asymmetric PWM:

$$\text{TxPR Value} = \left[\frac{\textit{desired PWM period}}{\textit{GP Timer prescaled clk period}} - 1 \right] \tag{6.1}$$

Symmetric PWM:

$$\text{TxPR Value} = \left\lceil \frac{\textit{desired PWM period}}{2 * (\textit{GP Timer prescaled clk period})} \right\rceil \quad (6.2)$$

5. Initialize TxCMPR to first desired compare value
6. To create a PWM signal, the registers GPTCONA/B and TxCON need to be configured for TxCMP enabled, desired counting mode etc.
7. To create an asymmetric PWM signal, the timer is set to the Continuous-Up Count Mode. If a symmetric PWM signal is desired, then the Timer should be set to the Continuous-Up/Down Mode.
8. During run time, the GP Timer compare register (TxCMPR) will need to be periodically updated with new compare values corresponding to the modulation signal or new duty cycle. This can be done during an interrupt service routine.

Example 6.3 - Fixed Duty Cycle PWM

The following block of code is an example of generating a simple fixed-duty cycle PWM signal by using the GP Timer Compare function. The PLL needs to be set to CLKIN x 4, the watchdog needs to be disabled, and the wait state generator (WSGR) set for zero wait states.

```
LDP     #SCSR1>>7
        SPLK    #000Ch,SCSR1    ;EVA & EVB modules clock enable
        LDP     #0E1h           ;Set Mux pins for
        SPLK    #0FFFFh,MCRA    ;PWM function
        SPLK    #0FFFFh,MCRC    ;EVA PWM output initialization
        LDP     #GPTCONA >> 7h ;Load EVA data-page
        SPLK    #00000h, T1CNT ;this just zeros the counter T1 the
                                ;counters are auto zeroed after a DSP
                                ;reset
        SPLK    #0FFFFh, T1PR  ;the T1PR value sets the frequency in
                                ;this case, it is 500 Hz cont up-cnt mod
        SPLK    #08000h, T1CMPR ;50 % duty cycle PWM bits---
        SPLK    #0000000001000010b, GPTCONA
        SPLK    #1001000001000010b, T1CON
LOOP2   B       LOOP2           ;after the control registers are setup
                                ;the program can loop endlessly while
                                ;PWM is generated automatically
```

6.4 Compare Units

A PWM signal can also be generated using the compare unit (CMPRx). The compare units (CMPRx) in the LF2407 function identically to the GP Timer compare units (TxCMPR) discussed above. Unlike the GP Timer compare function, each compare unit has *two* associated PWM outputs which both toggle on

the same compare match. The PWM outputs associated with the compare units allow for the generation of six PWM outputs per EV.

As shown in Fig. 6.10 the Compare Units Include:

- Three 16-bit compare registers (CMPR1, CMPR2, and CMPR3 for EVA; and CMPR4, CMPR5, and CMPR6 for EVB), all double-buffered
- One 16-bit compare control register (COMCONA for EVA, and COM-CONB for EVB)
- One 16-bit action control register (ACTRA for EVA, and ACTRB for EVB), with an associated buffer register
- Six PWM (3-state; Low, High, High Z) output (compare output) pins (PWMy, y = 1, 2, 3, 4, 5, 6 for EVA and PWMz, z = 7, 8, 9, 10, 11, 12 for EVB)

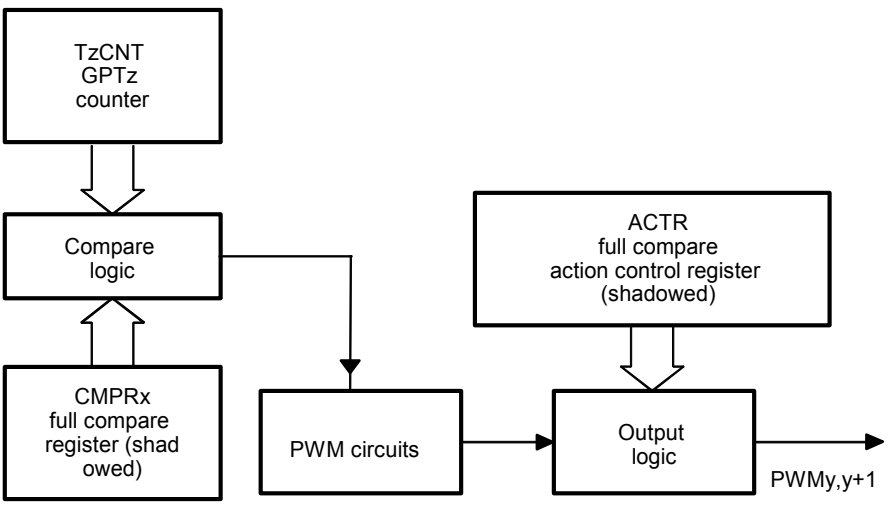

Figure 6.10 Compare unit block diagram.

For EVA: x = 1, 2, 3; y = 1, 3, 5; z = 1

For EVB: x = 4, 5, 6; y = 7, 9, 11; z = 3

6.4.1 Inputs and Outputs of the Compare Units

The inputs to a compare unit include:

- Control signals from compare control registers
- GP Timer 1/3 (T1CNT/T3CNT) count value, underflow, and period match signals
- System RESET
- The time base (counter value) for the compare units in EVA (CMPR1,2 ,3) is GP Timer 1, and for EVB (CMPR4, 5, 6) is GP Timer 3.

When any reset event occurs, all register bits associated with the compare units are reset to zero and all compare output pins are put in the high-impedance state.

The output of a compare unit is a compare match output, or in other words, a PWM output. If the compare operation is enabled, a compare match signal sets the corresponding interrupt flag and the two output pins associated with the compare unit to toggle. Either of the two outputs can be configured as either active high or active low, but will toggle upon the same event.

6.4.2 Operation of Compare Units

The sequence below is an example of the compare unit operation in EVA. For EVB operation, GP Timer 3 and ACTRB are used instead:

1. The value of the GP Timer 1 counter is continuously compared with that of the compare register.
2. When a compare match occurs, a transition appears on the two outputs of the compare unit according to the bits in the action control register (ACTRA). The bits in the ACTRA can individually specify each output to toggle active high or toggle active-low (if not forced high or low) on a compare match.
3. The compare interrupt flag associated with a compare unit is set when a compare match is made between GP Timer 1 and the compare register of a compare unit, if compare is enabled.
4. A peripheral interrupt request will then be generated if the interrupt is unmasked. The timing of output transitions, setting of interrupt flags, and the generation of interrupt requests are similar to the GP Timer compare operation.
5. The outputs of the compare units in compare mode are subject to modification by the output logic, dead band units, and the space vector PWM logic.

Having two outputs controlled by the same compare unit is useful in applications such as the control of a power inverter (see Fig. 6.11). With a power inverter, PWM signals can be used to gate the power transistors for creating currents through the legs of the inverter of any frequency or amplitude. This is useful in controlling electric motors their operation depends on the current flowing through the windings. By controlling the current flowing through motor windings, torque and speed control of the motor can be accomplished.

In inverter circuits such as those shown in Fig. 6.11, two power transistors are placed in series on each phase “leg” with the output being between them. This allows the output of the leg to be connected either to the DC supply voltage (Vdc) or ground. A potential hazard with these circuits is that if both transistors are turned on at the same time, a short circuit condition will exist through the leg and power transistors, causing the transistors to rapidly heat up and, in most cases, explode.

The solution to this problem is to make sure that only one transistor in each leg is on at a time. In theory, this is accomplished by feeding complementary PWM gating signals to each of the two transistors in a leg. So when one transistor is on, the other is off. In reality, all transistors turn on faster than they turn off. Therefore, it is necessary to add a time delay (dead-band) between the PWM signals to allow for the first transistor to fully turn off before the second one is turned on.

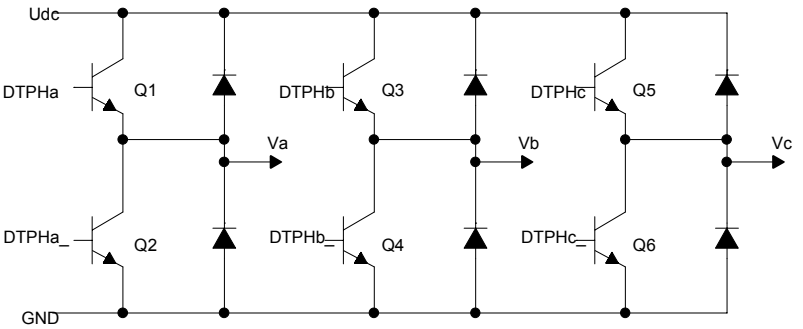

Figure 6.11 Basic three-phase inverter circuit.

6.4.3 Dead Band Generation

Unlike the GP Timer Compare PWM generation, the compare unit PWM outputs allow for a programmable dead band. Each EV on the LF2407 has its own programmable dead-band unit. The dead-band generators generate the dead-band delay between the toggling of the independent and dependent PWM outputs. Dead band solves the problem of inverter leg shoot through (short circuits). Figure 6.12 shows the interconnection between the dead band units and the compare units.

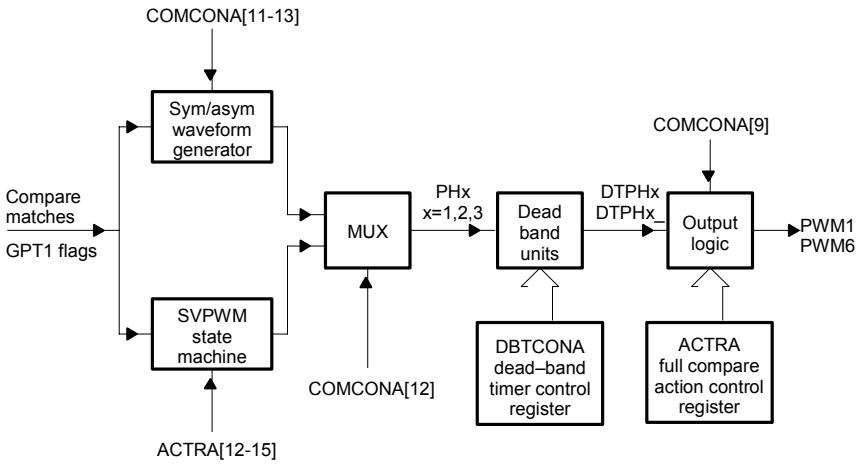

Figure 6.12 Block diagram of PWM outputs showing dead-band units.

Each programmable dead-band unit features:

- One 16-bit dead-band control register, DBTCONx (RW)
- One input clock prescaler: x/1, x/2, x/4, etc., to x/32
- Device (CPU) clock input
- Three 4-bit down-counting timers
- Control logic

Figures 6.13 and 6.14 illustrate the addition of a dead-band in both asymmetric and symmetric PWM outputs. The toggling sequence might go as follows: (1) toggle first output, (2) delay for a certain "dead-band" of clock cycles, (3) toggle the second output pin. This addition of a proper amount of dead-band prevents a short circuit across an inverter leg.

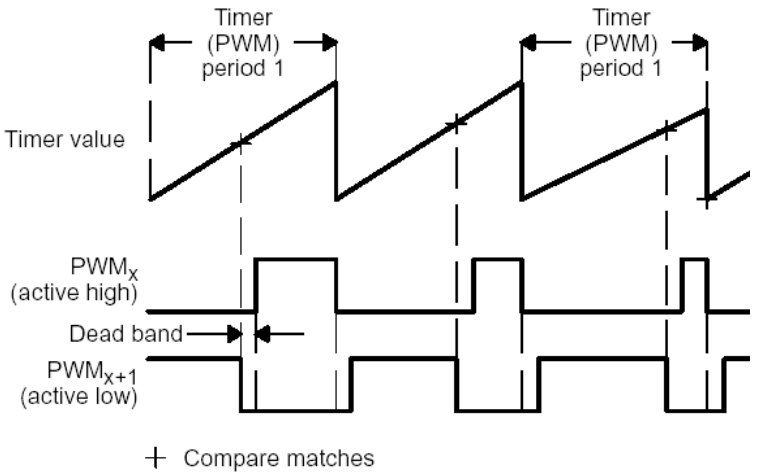

Figure 6.13 Dead-band with an asymmetric PWM output.

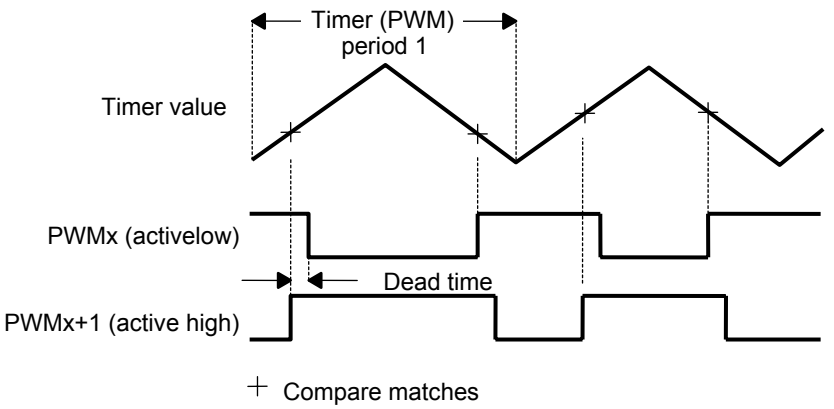

Figure 6.14 Dead-band with an asymmetric PWM output.

Depending on the switching device used, more or less dead-band might be needed. The use of dead-band should be experimented with when the inverter is supplied at a very low power level. This will ensure that if the current dead-band value is not sufficient, then the switching devices will not incur damage from the limited shoot through.

Table 6.4 lists the amounts of dead-band generated by the different bit combinations in DBTCONx. The values are based on a 25ns input clock signal. We can calculate the dead-band generated by the following simple formula:

$$\text{Dead Band (\# of CPU clock cycles)} = \frac{bits\ [8 \rightarrow 11]\ in\ DBTCONx}{clock\ \ prescale\ value}$$

Table 6.4 Dead-Band Values Generated by Bits [8 through 11] in DBTCONx Register

	(DBTCONx bits [4–2])					
DBTCONx bits [11–8]	110 and 1x1 (P=32)	100 (P=16)	011 (P=8)	010 (P=4)	001 (P=2)	000 (P=1)
0	0	0	0	0	0	0
1	0.8	0.4	0.2	0.1	0.05	0.025
2	1.6	0.8	0.4	0.2	0.1	0.05
3	2.4	1.2	0.6	0.3	0.15	0.075
4	3.2	1.6	0.8	0.4	0.2	0.1
5	4	2	1	0.5	0.25	0.125
6	4.8	2.4	1.2	0.6	0.3	0.15
7	5.6	2.8	1.4	0.7	0.35	0.175
8	6.4	3.2	1.6	0.8	0.4	0.2
9	7.2	3.6	1.8	0.9	0.45	0.225
A	8	4	2	1	0.5	0.25
B	8.8	4.4	2.2	1.1	0.55	0.275
C	9.6	4.8	2.4	1.2	0.6	0.3
D	10.4	5.2	2.6	1.3	0.65	0.325
E	11.2	5.6	2.8	1.4	0.7	0.35
F	12	6	3	1.5	0.75	0.375

Note: *Table values are given in μs.*

6.4.4 Register Setup for Compare Unit Operation

The following sequence should be used in setting up the Event Manager (EVA/B) for compare (PWM generation) operation:

EVA:

1. Set the T1PR for the desired period.
2. Configure ACTRA to select compare actions.
3. Configure DBTCONA, if dead band is to be used.
4. Initialize CMPRx to the first compare value.
5. Configure COMCONA for desired operation.
6. Configure T1CON to produce the desired operation for the time base and start the operation.
7. Load new compare values into CMPRx during program.

EVB:

1. Set the T3PR for the desired counting period.
2. Configure ACTRB to select compare actions.
3. Configure DBTCONA, if dead band is to be used.
4. Initialize CMPRx to the first compare value.
5. Configure COMCONB for desired operation.
6. Configure T3CON to produce the desired operation for the time base.
7. Load new compare values into CMPRx during program.

6.4.5 Compare Unit Interrupts

There is a maskable interrupt flag in EVIFRA and EVIFRC for each compare unit. If a compare operation is enabled, the interrupt flag of a compare unit is set one clock cycle after a compare match. A peripheral interrupt request will also be generated by the flag bit if the flag is unmasked.

6.4.6 Data Memory Mapped Registers Associated with the Compare Units

There are six main registers that control the functionality of the compare units on the LF2407: COMCONA/B, ACTRA/B, and DBTCONA/B. In addition to the control registers described in this section, the GP Timer registers should be thought of as being included because they provide the count value or time base in which the compare units operate.

Compare Control Registers (COMCONA and COMCONB)

These registers (COMCONA and COMCONB) control the operation of the compare units. They determine whether the compare operation is enabled, whether the compare outputs are enabled, the condition on which the compare registers are updated with the values in their buffer registers, and whether the Space Vector PWM (SVPWM) mode is enabled.

Compare Control Register A (COMCONA) — Address 7411h

15	14	13	12	11	10	9	8
CENABLE	CLD1	CLD0	SVENABLE	ACTRLD1	ACTRLD0	FCOMPOE	$\overline{PDPINTA}$ STATUS
RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	R– $\overline{PDPINTA}$ PIN
7-0							
Reserved							
R–0							

Note: *R = read access, W = write access, -0 = value after reset.*

Bit 15 **CENABLE**. Compare enable.
- 0 Disables compare operation. All shadowed registers (CMPRx, ACTRA) become transparent
- 1 Enables compare operation

Bits14–13 **CLD1, CLD0**. Compare register CMPRx reload condition.
- 00 When T1CNT = 0 (that is, on underflow)
- 01 When T1CNT = 0 or T1CNT = T1PR (that is, on underflow or period match)
- 10 Immediately
- 11 Reserved; result is unpredictable

Bit 12 **SVENABLE**. Space vector PWM mode enable.
- 0 Disables space vector PWM mode
- 1 Enables space vector PWM mode

Bits 11–10 **ACTRLD1, ACTRLD0**. Action control register reload condition.
- 00 When T1CNT = 0 (on underflow)
- 01 When T1CNT = 0 or T1CNT = T1PR (on underflow or period match)
- 10 Immediately
- 11 Reserved

Bit 9 **FCOMPOE**. Compare output enable. Active PDPINTA clears this bit to zero.
- 0 PWM output pins are in high-impedance state; that is, they are disabled
- 1 PWM output pins are not in high-impedance state; that is, they are enabled

Bit 8 **PDPINTA STATUS**. This bit reflects the current status of the PDPINTA pin. (This bit is applicable to 240xA devices only — it is reserved on 240x devices and returns a zero when read.)

Bits 7–0 **Reserved**. Read returns zero; writes have no effect.

Compare Control Register B (COMCONB) — Address 7511h

15	14	13	12	11	10	9	8
CENABLE	CLD1	CLD0	SVENABLE	ACTRLD1	ACTRLD0	FCOMPOE	$\overline{PDPINTB}$ STATUS
RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	R– $\overline{PDPINTB}$ PIN
7-0							
Reserved							
R–0							

Note: *R = read access, W = write access, -0 = value after reset.*

Bit 15 **CENABLE**. Compare enable.
- 0 Disable compare operation. All shadowed registers (CMPRx, ACTRB) become transparent
- 1 Enable compare operation

Bits14–13 **CLD1, CLD0**. Compare register CMPRx reload condition.
- 00 When T3CNT = 0 (that is, on underflow)
- 01 When T3CNT = 0 or T3CNT = T3PR (that is, on underflow or period match)
- 10 Immediately
- 11 Reserved; result is unpredictable

Bit 12 **SVENABLE**. Space vector PWM mode enable.
- 0 Disables space vector PWM mode
- 1 Enables space vector PWM mode

Bits 11–10 **ACTRLD1, ACTRLD0**. Action control register reload condition.
- 00 When T3CNT = 0 (on underflow)
- 01 When T3CNT = 0 or T3CNT = T3PR (on underflow or period match)
- 10 Immediately
- 11 Reserved

Bit 9 **FCOMPOE**. Compare output enable. Active PDPINTB clears this bit to zero.
- 0 PWM output pins are in high-impedance state; that is, they are disabled
- 1 PWM output pins are not in high-impedance state; that is, they are enabled

Bit 8 **PDPINTB STATUS**. This bit reflects the current status of the PDPINTB pin. (This bit is applicable to 240xA devices only — it is reserved on 240x devices and returns a zero when read.)

Bits 7–0 **Reserved**. Read returns zero; writes have no effect.

Compare Action Control Registers (ACTRA and ACTRB)

The double buffered, compare action control registers (ACTRA and ACTRB) determine what action occurs on each of the six compare output pins when a compare event occurs (if the compare operation is enabled by COMCONx[15]). The compare output pins are PWMx, where x = 1–6 for ACTRA, and x = 7–12 for ACTRB. The condition on which ACTRA and ACTRB are reloaded is defined by the bits in COMCONx.

Compare Action Control Register A (ACTRA) — Address 7413h

15	14	13	12	11	10	9	8
SVRDIR	D2	D1	D0	CMP6ACT1	CMP6ACT0	CMP5ACT1	CMP5ACT0
RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0
7	6	5	4	3	2	1	0
CMP4ACT1	CMP4ACT0	CMP3ACT1	CMP3ACT0	CMP2ACT1	CMP2ACT0	CMP1ACT1	CMP1ACT0
RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

Note: *R = read access, W = write access, -0 = value after reset.*

Bit 15 **SVRDIR**. Space vector PWM rotation direction. Used only in space vector PWM output generation.
0 Positive (CCW)
1 Negative (CW)

Bits 14–12 **D2–D0**. Basic space vector bits. Used only in space vector PWM output generation.

Bits 11–10 **CMP6ACT1–0**. Action on compare output pin 6, CMP6.
00 Forced low
01 Active low
10 Active high
11 Forced high

Bits 9–8 **CMP5ACT1–0**. Action on compare output pin 5, CMP5.
00 Forced low
01 Active low
10 Active high
11 Forced high

Bits 7–6 CMP4ACT1–0. Action on compare output pin 4, CMP4.
- 00 Forced low
- 01 Active low
- 10 Active high
- 11 Forced high

Bits 5–4 CMP3ACT1–0. Action on compare output pin 3, CMP3.
- 00 Forced low
- 01 Active low
- 10 Active high

Bits 3–2 CMP2ACT1–0. Action on compare output pin 2, CMP2.
- 00 Forced low
- 01 Active low
- 10 Active high
- 11 Forced high

Bits 1–0 CMP1ACT1–0. Action on compare output pin 1, CMP1.
- 00 Forced low
- 01 Active low
- 10 Active high
- 11 Forced high

Compare Action Control Register B (ACTRB) — Address 7513h

15	14	13	12	11	10	9	8
SVRDIR	D2	D1	D0	CMP12ACT1	CMP12ACT0	CMP11ACT1	CMP11ACT0
RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0
7	6	5	4	3	2	1	0
CMP10ACT1	CMP10ACT0	CMP9ACT1	CMP9ACT0	CMP8ACT1	CMP8ACT0	CMP7ACT1	CMP7ACT0
RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	RW–0

Note: *R = read access, W = write access, -0 = value after reset.*

Bit 15 SVRDIR. Space vector PWM rotation direction. Used only in space vector PWM output generation.
- 0 Positive (CCW)
- 1 Negative (CW)

Bits 14–12 D2–D0. Basic space vector bits. Used only in space vector PWM output generation.

Bits 11–10 CMP12ACT1–0. Action on compare output pin 12, CMP12.
- 00 Forced low
- 01 Active low

10 Active high
11 Forced high

Bits 9–8 CMP11ACT1–0. Action on compare output pin 11, CMP11.
00 Forced low
01 Active low
10 Active high
11 Forced high

Bits 7–6 CMP10ACT1–0. Action on compare output pin 10, CMP10.
00 Forced low
01 Active low
10 Active high
11 Forced high

Bits 5–4 CMP9ACT1–0. Action on compare output pin 9, CMP9.
00 Forced low
01 Active low
10 Active high
11 Forced high

Bits 3–2 CMP8ACT1–0. Action on compare output pin 8, CMP8.
00 Forced low
01 Active low
10 Active high
11 Forced high

Bits 1–0 CMP7ACT1–0. Action on compare output pin 7, CMP7.
00 Forced low
01 Active low
10 Active high
11 Forced high

Dead-Band Timer Control Register A (DBTCONA) — Address 7415h

15-12				11	10	9	8
Reserved				DBT3	DBT2	DBT1	DBT0
R–0				RW–0	RW–0	RW–0	RW–0
7	6	5	4	3	2	1-0	
EDBT3	EDBT2	EDBT1	DBTPS2	DBTPS1	DBTPS0	Reserved	
RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	R–0	

Note: *R = read access, W = write access, -0 = value after reset.*

Bits 15–12 Reserved. Reads return zero; writes have no effect.

Bits 11–8 DBT3 (MSB)–DBT0 (LSB). Dead-band timer period. These bits define the period value of the three 4-bit dead-band timers.

Bit 7 **EDBT3**. Dead-band timer 3 enable (for pins PWM5 and PWM6 of Compare Unit 3).
0 Disable
1 Enable

Bit 6 **EDBT2**. Dead-band timer 2 enable (for pins PWM3 and PWM4 of Compare Unit 2).
0 Disable
1 Enable

Bit 5 **EDBT1**. Dead-band timer 1 enable (for pins PWM1 and PWM2 of Compare Unit 1).
0 Disable
1 Enable

Bits 4–2 DBTPS2 to DBTPS0. Dead-band timer prescaler.
000 x/1
001 x/2
010 x/4
011 x/8
100 x/16
101 x/32
110 x/32
111 x/32
x = Device (CPU) clock frequency

Bits 1–0 Reserved. Reads return zero; writes have no effect.

Dead-Band Timer Control Register B (DBTCONB) — Address 7515h

15-12				11	10	9	8
Reserved				DBT3	DBT2	DBT1	DBT0
R–0				RW–0	RW–0	RW–0	RW–0
7	6	5	4	3	2	1-0	
EDBT3	EDBT2	EDBT1	DBTPS2	DBTPS1	DBTPS0	Reserved	
RW–0	RW–0	RW–0	RW–0	RW–0	RW–0	R–0	

Note: *R = read access, W = write access, -0 = value after reset.*

Bits 15–12 Reserved. Reads return zero; writes have no effect.

Bits 11–8 **DBT3 (MSB)–DBT0 (LSB)**. Dead-band timer period. These bits define the period value of the three 4-bit dead-band timers.

Bit 7 **EDBT3**. Dead-band timer 3 enable (for pins PWM11 and PWM12 of Compare 6).
0 Disable
1 Enable

Bit 6 **EDBT2**. Dead-band timer 2 enable (for pins PWM9 and PWM10 of Compare 5).
0 Disable
1 Enable

Bit 5 **EDBT1**. Dead-band timer 1 enable (for pins PWM7 and PWM8 of Compare 4).
0 Disable
1 Enable

Bits 4–2 DBTPS2 to DBTPS0. Dead-band timer prescaler.
000 x/1
001 x/2
010 x/4
011 x/8
100 x/16
101 x/32
110 x/32
111 x/32
x = Device (CPU) clock frequency

Bits 1–0 Reserved. Reads return zero; writes have no effect.

6.5 Capture Units and Quadrature Encoded Pulse (QEP) Circuitry

The Capture Units on the LF2407 allow an event (rising/falling edge) on the capture pin to be time stamped by a selected GP Timer. There are three Capture Units in each EV, each with its own capture input pin (CAPx). Capture Units 1, 2, and 3 are associated with EVA while Capture Units 4, 5, and 6 are associated with EVB. Each EV module contains the following (shown in Figs. 6.14 and 6.15):

- One 16 bit capture control register per EV (CAPCOMA for EVA, CAPCOMB for EVB) is used for configuring the Capture Unit functionality.
- Three 16-bit, 2-level-deep First-In-First-Out (FIFO) stacks per EV (CAPxFIFO); one FIFO stack for each Capture Unit; the "captured" timer count value is stored here.
- One 16-bit capture status register (CAPFIFOA for EVA, CAPFIFOB for EVB); provides information on the number of timer captures in each capture FIFO.

- Inputs of either GP Timer 1 or 2 (for EVA) and GP Timer 3 or 4 (for EVB) as the time base.
- One capture pin per Capture Unit with user-specified transition detection (rising edge, falling edge, or both edges). CAP1 through CAP3 for EVA, and CAP4 through CAP6 for EVB.
- Six maskable interrupt flags, one for each Capture Unit.

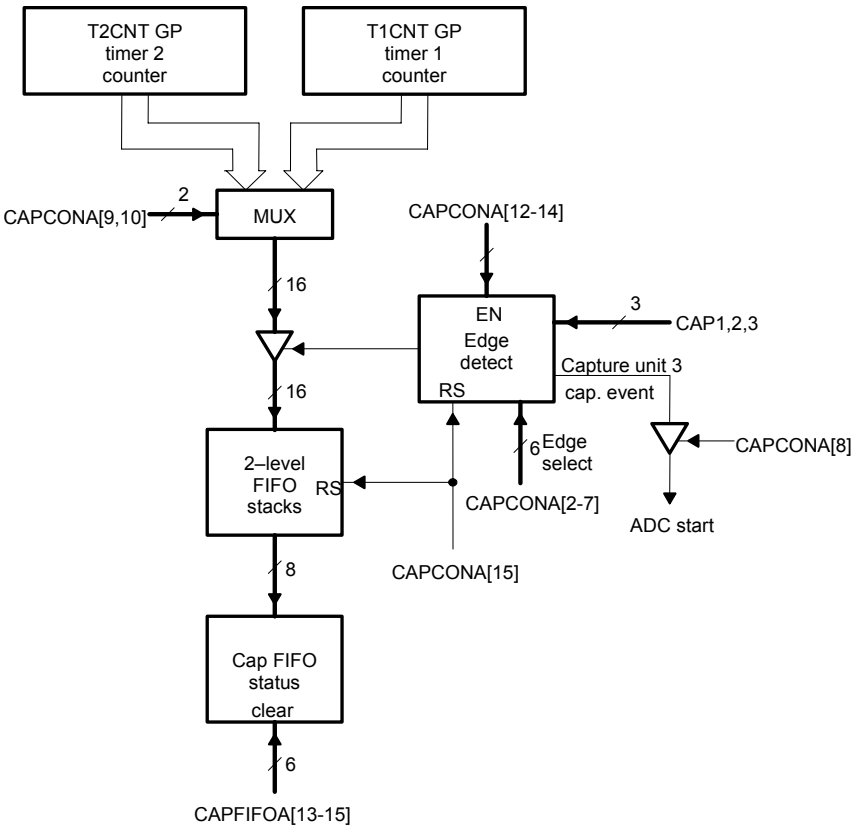

Figure 6.15 EVA capture unit diagram. (Courtesy of Texas Instruments)

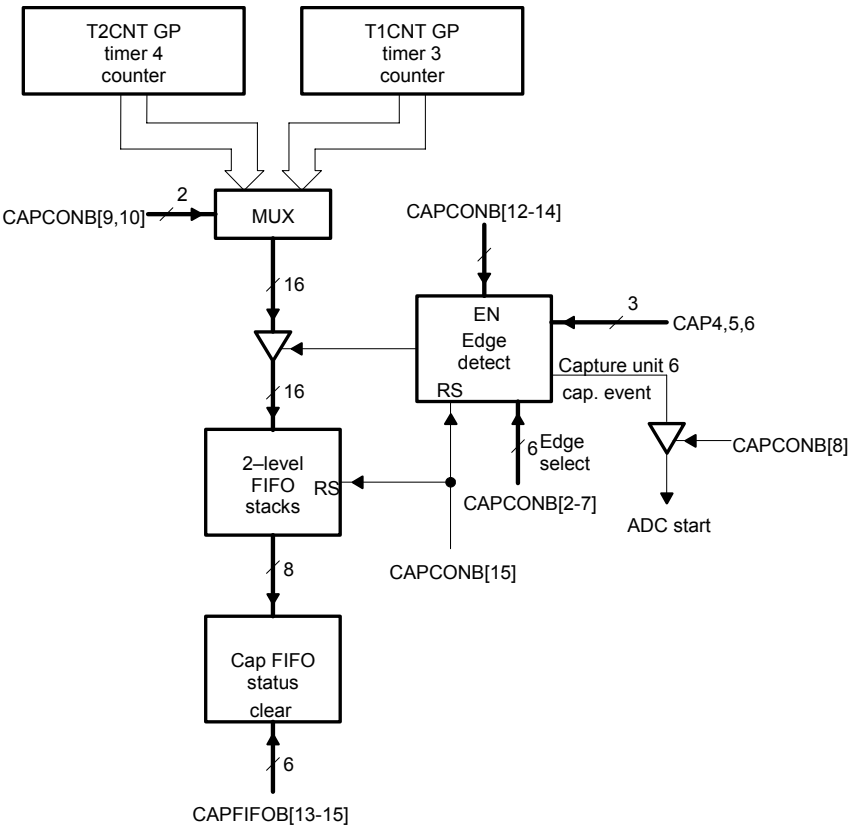

Figure 6.16 EVB Capture unit diagram. (Courtesy of Texas Instruments)

The Capture Units are useful in applications where the time of an external trigger needs to be "captured". For example, if we want to measure the time between the rising edges of two pulses, we would configure the appropriate registers for capture operation on a specific capture pin. At each rising edge, the Capture Unit would then store the corresponding timer values. The user program could then subtract the second capture value from the first value and determine the time between the pulses.

The Capture Units are accompanied by the Quadrature Encoded Pulse (QEP) circuitry which uses the GP Timers to "decode" a QEP signal. When the QEP mode is selected, pins CAP1 and CAP2 (CAP4 and CAP5 in case of EVB) are used as QEP inputs. More on the QEP circuitry will be discussed shortly.

6.5.1 Operation of the Capture Unit

When a Capture Unit is enabled, when either a rising or falling edge is detected on the capture input pin (CAPx), the current value of the selected GP Timer counter is copied and stored in the corresponding capture FIFO. In order for a transition to be captured, the input must hold at its current level for the duration of at least two CPU clock cycles. After the GP Timer value is recorded in the capture FIFO, an interrupt could also be generated, and software may then read the FIFO value. The value from the capture FIFO can then be used in an algorithm.

While we can think of the capture FIFO as being a two-level deep single register, each capture FIFO stack actually consists of two registers, CAPxFIFO and CAPxBOT (for EVA x=1,2,3; EVB x=4,5,6). When a new value is stored in the FIFO during a capture, in reality it first goes to the bottom register. When the top register of the FIFO stack is empty (either because this is the first capture, or the FIFO was just read), the value in the bottom register is automatically shifted into the top register (CAPxFIFO). Because of the above operation, when reading from the FIFO, the FIFO will always return the oldest stored value first. When the FIFO contains two values and is read, the oldest value will be read and removed from the FIFO. On the next read, the next oldest value will be read and removed from the FIFO. Usually, only read from the CAPxFIFO register, but the bottom register of the stack (CAPxBOT) can also be read.

When no FIFO reads have been performed, after two captures the corresponding capture FIFO will have two timer values stored in it and will be full. In the case that the FIFO has still not been read from and a third capture is recorded, the first capture value will be pushed out of the FIFO and lost.

The bits in the FIFO status registers indicate how many values are currently stored in each FIFO. When a value is read from the CAPxFIFO (or bottom register, CAPxBOT), the status bits will indicate one less value in the FIFO. The two status bits corresponding to a particular FIFO should normally indicate “00”, “01”, and “10”. If a third capture occurs and the previous two values have not been read from the FIFO, the status bits will indicate “11”, indicating that the oldest value was lost. In this case, after the next FIFO read, the status bits return to their usual values of “00”, “01” or “10”.

The following steps should be taken to configure the Capture Units for operation:

1. Initialize the CAPFIFOx and clear the appropriate status bits.
2. Set the selected GP Timer in the desired counting mode.
3. Set the associated GP Timer compare register or GP Timer period register, if necessary.
4. Set up CAPCONA or CAPCONB as appropriate for desired operation.

6.5.2 Capture Stack Interrupt Flag Operation:

Because the FIFO stack is two levels deep, the corresponding interrupt flag is set as soon as there are two values in the stack (the FIFO is full). This means that if there is one (or two) previous values in the FIFO (indicated by CAPxFIFO bits not equal to zero) and another capture takes place, the interrupt flag will be set. Like all interrupts, if the flag is unmasked, then an interrupt is generated. If interrupt operation is not desired, either the interrupt flag or the status bits can be polled continuously to determine if capture events have occurred.

6.5.3 Quadrature Encoded Pulse (QEP) Circuitry

QEPs are two sequences of pulses which have a variable frequency and are 90º out of phase with one another (see Fig. 6.17). QEP signals are usually generated by a position/speed sensing device such as a rotary optical encoder. When the encoder is rotated, the direction of rotation can be determined by which sequence of pulses leads the other. Rotational speed and position can be determined from the count and frequency of the pulses.

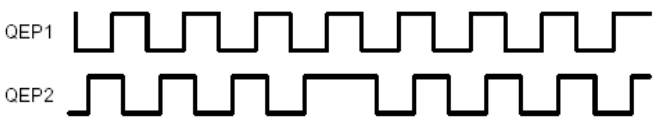

Figure 6.17 A pair of quadrature encoded pulses.

Each EV module has a QEP circuit associated with the Capture Units (see Figs. 6.18 and 6.19). The QEP circuit, when enabled, decodes and counts the quadrature encoded input pulses on the QEP input pins. The input pins consist of CAP1/QEP1 and CAP2/QEP2 for EVA or CAP4/QEP3 and CAP5/QEP4 for EVB. When the QEP function is enabled, the compare function of the pins is disabled and the pins are configured for QEP input.

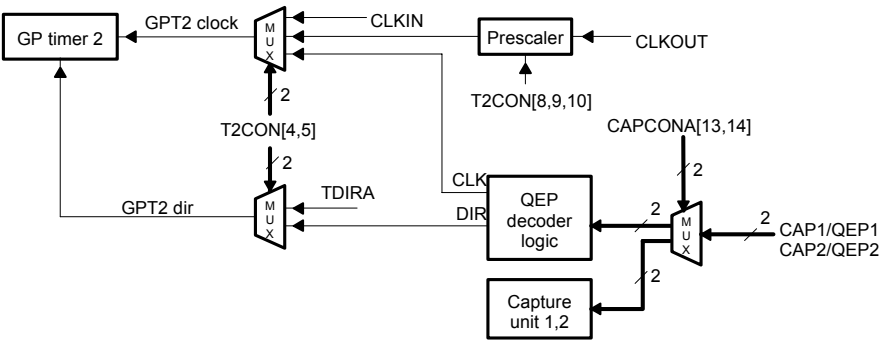

Figure 6.18 QEP circuit block for EVA. (Courtesy of Texas Instruments)

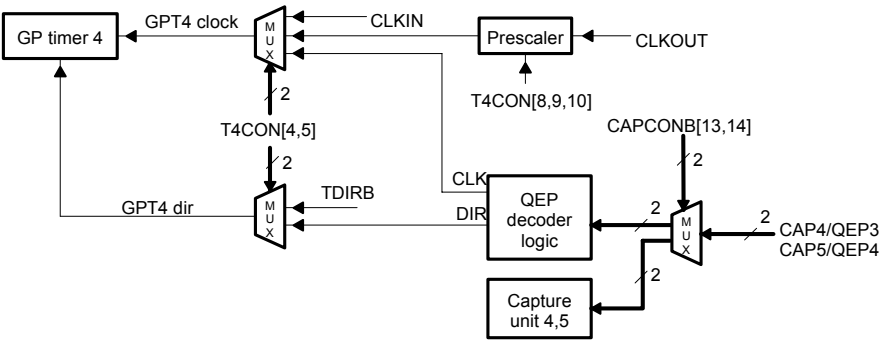

Figure 6.19 QEP circuit for EVB. (Courtesy of Texas Instruments)

QEP Circuit Operation

The counter for the QEP circuit is provided by GP Timer 2 for EVA and GP Timer 4 for EVB. The GP Timer must be configured for directional-up/down count mode. When the QEP circuit is selected as the clock source, the timer ignores the direction and clock (TDIRA/B and TCLKINA/B) input pins. The QEP circuit will act as the clock reference and the direction input for the timer. The QEP circuit determines which one of the sequences is the leading sequence. It then generates a direction signal as the direction input to the GP Timer. The timer counts up if CAP1/QEP1 (CAP4/QEP3 for EVB) input is the leading sequence, and counts down if CAP2/QEP2 (CAP5/QEP4 for EVB) is the leading sequence. Both edges of the pulses of the two quadrature encoded inputs are counted by the QEP circuit. Therefore, the frequency of the clock generated by the QEP logic to GP Timer 2 (or 4) is four times that of each input sequence. This quadrature clock is connected to the clock input of GP Timer 2 (or 4).

Note: *Upon a DSP RESET, the QEP logic will miss the first QEP edge.*

Configuring for QEP Operation:

EVA:

1. Load GP Timer 2's counter, period, and compare registers if desired; for simple QEP decoding, this is not required.
2. Configure T2CON to set GP Timer 2 in directional-up/down mode with the QEP circuits as clock source, and enable the selected timer.
3. Configure CAPCONA to enable the QEP circuit.

EVB:

1. Load GP Timer 4's counter, period, and compare registers with desired values; for simple QEP decoding, this is not required.
2. Configure T4CON to set GP Timer 4 in directional-up/down mode with the QEP circuits as clock source, and enable the selected timer.
3. Configure CAPCONB to enable the QEP circuit.

Interrupt flags normally associated with the timer operation are still operational with the QEP. Period, underflow, overflow, and compare interrupt flags for a GP Timer with a QEP circuit clock are generated on respective matches. If the respective interrupt flags are unmasked, timer interrupt requests will be generated.

6.5.4 Capture Unit / QEP Control Registers

Upon a RESET, all capture registers are cleared to zero. There are four 16-bit registers that control the functionality of the Capture Units. These registers are CAPCONA, CAPCONB, CAPFIFOA, and CAPFIFOB. In addition to these four registers the individual timer control registers (TxCON, x = 1, 2, 3, or 4) control the selected timer which acts as the time base for the Capture Unit. CAPCONA and CAPCONB also control the QEP functionality.

Capture Control Register A (CAPCONA) — Address 7420h

15	14-13	12	11	10	9	8
CAPRES	CAPQEPN	CAP3EN	Reserved	CAP3TSEL	CAP12TSEL	CAP3TOADC
RW–0	RW–0	RW–0	R–0	RW–0	RW–0	RW–0

7-6	5-4	3-2	1-0
CAP1EDGE	CAP2EDGE	CAP3EDGE	Reserved
RW–0	RW–0	RW–0	R–0

Note: *R = read access, W = write access, -0 = value after reset.*

Bit 15 **CAPRES**. Capture reset. Always reads zero.
Note: This bit is not implemented as a register bit. Writing a 0 simply clears the capture registers.
0 Clear all registers of Capture Units and QEP circuit to 0
1 No action

Bits 14–13 **CAPQEPN**. Capture Units 1 and 2 control.
00 Disables Capture Units 1 and 2; FIFO stacks retain their contents
01 Enables Capture Units 1 and 2
10 Reserved
11 Reserved

Bit 12 **CAP3EN**. Capture Unit 3 control.
- 0 Disables Capture Unit 3; FIFO stack of Capture Unit 3 retains its contents
- 1 Enable Capture Unit 3

Bit 11 **Reserved**. Reads return zero; writes have no effect.

Bit 10 **CAP3TSEL**. GP Timer selection for Capture Unit 3.
- 0 Selects GP Timer 2
- 1 Selects GP Timer 1

Bit 9 **CAP12TSEL**. GP Timer selection for Capture Units 1 and 2.
- 0 Selects GP Timer 2
- 1 Selects GP Timer 1

Bit 8 **CAP3TOADC**. Capture Unit 3 event starts ADC.
- 0 No action
- 1 Starts ADC when the CAP3INT flag is set

Bits 7–6 **CAP1EDGE**. Edge detection control for Capture Unit 1.
- 00 No detection
- 01 Detects rising edge
- 10 Detects falling edge
- 11 Detects both edges

Bits 5–4 **CAP2EDGE**. Edge detection control for Capture Unit 2.
- 00 No detection
- 01 Detects rising edge
- 10 Detects falling edge
- 11 Detects both edges

Bits 3–2 **CAP3EDGE**. Edge detection control for Capture Unit 3.
- 00 No detection
- 01 Detects rising edge
- 10 Detects falling edge
- 11 Detects both edges

Bits 1–0 **Reserved**. Reads return zero; writes have no effect.

Capture Control Register B (CAPCONB) — Address 7520h

15	14-13	12	11	10	9	8
CAPRES	CAPQEPN	CAP6EN	Reserved	CAP6TSEL	CAP45TSEL	CAP6TOADC
RW–0	RW–0	RW–0	R–0	RW–0	RW–0	RW–0
7-6	5-4	3-2	1-0			
CAP4EDGE	CAP5EDGE	CAP6EDGE	Reserved			
RW–0	RW–0	RW–0	RW–0			

Note: *R = read access, W = write access, -0 = value after reset.*

Bit 15 **CAPRES**. Capture reset. Always reads zero.
Note: This bit is not implemented as a register bit. Writing a 0 simply clears the capture registers.
0 Clears all registers of Capture Units and QEP circuit to 0
1 No action

Bits 14–13 **CAPQEPN**. Capture Units 4 and 5 and QEP circuit control.
00 Disables Capture Units 4 and 5 and QEP circuit. FIFO stacks retain their contents
01 Enables Capture Units 4 and 5, disable QEP circuit
10 Reserved
11 Enables QEP circuit. Disable Capture Units 4 and 5; bits 4–7 and 9 are ignored

Bit 12 **CAP6EN**. Capture Unit 6 control.
0 Disables Capture Unit 6; FIFO stack of Capture Unit 6 retains its contents
1 Enables Capture Unit 6

Bit 11 **Reserved**. Reads return zero; writes have no effect.

Bit 10 **CAP6TSEL**. GP Timer selection for Capture Unit 6.
0 Selects GP Timer 4
1 Selects GP Timer 3

Bit 9 **CAP45TSEL**. GP Timer selection for Capture Units 4 and 5.
0 Selects GP Timer 4
1 Selects GP Timer 3

Bit 8 **CAP6TOADC**. Capture Unit 6 event starts ADC.
0 No action
1 Starts ADC when the CAP6INT flag is set

Bits 7–6 CAP4EDGE. Edge detection control for Capture Unit 4.
- 00 No detection
- 01 Detects rising edge
- 10 Detects falling edge
- 11 Detects both edges

Bits 5–4 CAP5EDGE. Edge detection control for Capture Unit 5.
- 00 No detection
- 01 Detects rising edge
- 10 Detects falling edge
- 11 Detects both edges

Bits 3–2 CAP6EDGE. Edge detection control for Capture Unit 6.
- 00 No detection
- 01 Detects rising edge
- 10 Detects falling edge
- 11 Detects both edges

Bits 1–0 Reserved. Reads return zero; writes have no effect.

Capture Status Registers

The ability to write to the CAPFIFOx registers can be used as a programming advantage. For example, if a "01" is written to the CAPnFIFO bits by user code, the EV module is led to believe that there is already an entry in the FIFO. Subsequently, every time the FIFO gets a new value, a capture interrupt will be generated. If a write occurs to the CAPnFIFOA status bits at the same time as they are being updated by hardware (because of a capture event), the user written data takes precedence.

Capture FIFO Status Register A (CAPFIFOA) — Address 7422h

15-14	13-12	11-10	9-8
Reserved	CAP3FIFO	CAP2FIFO	CAP1FIFO
R–0	RW–0	RW–0	RW–0
7-0			
Reserved			
R–0			

Note: *R = read access, W = write access, -0 = value after reset.*

Bits 15–14 Reserved. Reads return zero; writes have no effect.

Bits 13–12 CAP3FIFO. CAP3FIFO Status
- 00 Empty
- 01 Has one entry
- 10 Has two entries

11 Had two entries and captured another one; first entry has been lost

Bits 11–10 CAP2FIFO. CAP2FIFO Status
00 Empty
01 Has one entry
10 Has two entries
11 Had two entries and captured another one; first entry has been lost

Bits 9–8 CAP1FIFO. CAP1FIFO Status
00 Empty
01 Has one entry
10 Has two entries
11 Had two entries and captured another one; first entry has been lost

Bits 7–0 Reserved. Reads return zero; writes have no effect.

Capture FIFO Status Register B (CAPFIFOB) — Address 7522h

15-14	13-12	11-10	9-8
Reserved	CAP6FIFO	CAP5FIFO	CAP4FIFO
R–0	RW–0	RW–0	RW–0
7-0			
Reserved			
R–0			

Note: *R = read access, W = write access, -0 = value after reset.*

Bits 15–14 Reserved. Reads return zero; writes have no effect.

Bits 13–12 CAP6FIFO. CAP6FIFO Status
00 Empty
01 Has one entry
10 Has two entries
11 Had two entries and captured another one; first entry has been lost

Bits 11–10 CAP5FIFO. CAP5FIFO Status
00 Empty
01 Has one entry
10 Has two entries
11 Had two entries and captured another one; first entry has been lost

Bits 9–8 CAP4FIFO. CAP4FIFO Status
00 Empty
01 Has one entry
10 Has two entries
11 Had two entries and captured another one; first entry has been lost

Bits 7–0 **Reserved**. Reads return zero; writes have no effect.

6.6 General Event Manager Information

Table 6.5 Event Manager A (EVA) Pins

Pin Name	Description
CAP1/QEP1	Capture Unit 1 input, QEP circuit input 1
CAP2/QEP2	Capture Unit 2 input, QEP circuit input 2
CAP3	Capture Unit 3 input
PWM1	Compare Unit 1 output 1
PWM2	Compare Unit 1 output 2
PWM3	Compare Unit 2 output 1
PWM4	Compare Unit 2 output 2
PWM5	Compare Unit 3 output 1
PWM6	Compare Unit 3 output 2
T1CMP/T1PWM	Timer 1 compare/PWM output
T2CMP/T2PWM	Timer 2 compare/PWM output
TCLKINA	External clock-in for timers in EVA (*when configured to operate from external clock*)
TDIRA	External timer direction input in EVA (*when timer is in directional up/down mode*)

Table 6.6 Event Manager B (EVB) Pins

Pin Name	Description
CAP4/QEP3	Capture Unit 4 input, QEP circuit input 3
CAP5/QEP4	Capture Unit 5 input, QEP circuit input 4
CAP6	Capture Unit 6 input
PWM7	Compare Unit 4 output 1
PWM8	Compare Unit 4 output 2
PWM9	Compare Unit 5 output 1
PWM10	Compare Unit 5 output 2
PWM11	Compare Unit 6 output 1
PWM12	Compare Unit 6 output 2
T3CMP/T3PWM	Timer 3 compare/PWM output
T4CMP/T4PWM	Timer 4 compare/PWM output
TCLKINB	External clock-in for timers in EVB (*when configured to operate from external clock*)
TDIRB	External timer direction input in EVB (*when timer is in directional up/down mode*)

NOTE: *Most of the EV pins are mapped with a second function. In order to use the EV, you must configure the appropriate pins to their EV function. For more information on how pin sharing works and how to configure pins refer to Chapter 4.*

Event Manager (EV) Register Addresses

Table 6.7 Addresses of EVA Timer Registers

Address	Register	Name	
7400h	GPTCONA	GP Timer control register A	
7401h	T1CNT	Timer 1 counter register	Timer 1
7402h	T1CMPR	Timer 1 compare register	
7403h	T1PR	Timer 1 period register	
7404h	T1CON	Timer 1 control register	
7405h	T2CNT	Timer 2 counter register	
7406h	T2CMPR	Timer 2 compare register	Timer 2
7407h	T2PR	Timer 2 period register	
7408h	T2CON	Timer 2 control register	

Table 6.8 Addresses of EVB Timer Registers

Address	Register	Name	
7500h	GPTCONB	GP Timer control register B	
7501h	T3CNT	Timer 3 counter register	
7502h	T3CMPR	Timer 3 compare register	Timer 3
7503h	T3PR	Timer 3 period register	
7504h	T3CON	Timer 3 control register	
7505h	T4CNT	Timer 4 counter register	
7506h	T4CMPR	Timer 4 compare register	Timer 4
7507h	T4PR	Timer 4 period register	
7508h	T4CON	Timer 4 control register	

Table 6.9 Addresses of EVA Compare Control Registers

Address	Register	Name
7411h	COMCONA	Compare control register
7413h	ACTRA	Compare action control register
7415h	DBTCONA	Dead-band timer control register
7417h	CMPR1	Compare register 1
7418h	CMPR2	Compare register 2
7419h	CMPR3	Compare register 3

Table 6.10 Addresses of EVB Compare Control Registers

Address	Register	Name
7511h	COMCONB	Compare control register
7513h	ACTRB	Compare action control register
7515h	DBTCONB	Dead-band timer control register
7517h	CMPR4	Compare register 4
7518h	CMPR5	Compare register 5
7519h	CMPR6	Compare register 6

Table 6.11 Addresses of EVA Capture Registers

Address	Register	Name
7420h	CAPCONA	Capture control register
7422h	CAPFIFOA	Capture FIFO status register
7423h	CAP1FIFO	Two-level-deep capture FIFO stack 1
7424h	CAP2FIFO	Two-level-deep capture FIFO stack 2
7425h	CAP3FIFO	Two-level-deep capture FIFO stack 3
7427h	CAP1FBOT	Bottom registers of FIFO stacks; allows most recent CAPTURE value to be read
7428h	CAP2FBOT	
7429h	CAP3FBOT	

Table 6.12 Addresses of EVB Capture Registers

Address	Register	Name
7520h	CAPCONB	Capture control register
7522h	CAPFIFOB	Capture FIFO status register
7523h	CAP4FIFO	Two-level-deep capture FIFO stack 4
7524h	CAP5FIFO	Two-level-deep capture FIFO stack 5
7525h	CAP6FIFO	Two-level-deep capture FIFO stack 6
7527h	CAP4FBOT	Bottom registers of FIFO stacks, allows most recent CAPTURE value to be read
7528h	CAP5FBOT	
7529h	CAP6FBOT	

Table 6.13 Addresses of EVA Interrupt Registers

Address	Register	Name
742Ch	EVAIMRA	Interrupt mask register A
742Dh	EVAIMRB	Interrupt mask register B
742Eh	EVAIMRC	Interrupt mask register C
742Fh	EVAIFRA	Interrupt flag register A
7430h	EVAIFRB	Interrupt flag register B
7431h	EVAIFRC	Interrupt flag register C

Table 6.14 Addresses of EVB Interrupt Registers

Address	Register	Name
752Ch	EVBIMRA	Interrupt mask register A
752Dh	EVBIMRB	Interrupt mask register B
752Eh	EVBIMRC	Interrupt mask register C
752Fh	EVBIFRA	Interrupt flag register A
7530h	EVBIFRB	Interrupt flag register B
7531h	EVBIFRC	Interrupt flag register C

6.7 Exercise: PWM Signal Generation

As discussed in the previous sections, there are two ways to generate a PWM signal on the LF2407: through the GP Timer compare operation, or the Compare Units. This exercise will allow you to use your knowledge of the LF2407 DSP to write code that will generate PWM signals on both the GP Timer and Compare Unit outputs.

Procedure:

1. Write a program that outputs a fixed duty cycle "PWM" on a GP Timer 2 compare pin. Create the program so that the period of the PWM signal is 1 kHz and the duty cycle (on time/period) is fixed at 75%. The information on the GP Timer compare operation in the previous section will be very useful in writing this code.
2. View the output (1 kHz fixed duty cycle signal) on the T1PWM/T1CMP/IOPB4 pin. The Spectrum Digital LF2407 EVM schematic will be helpful in determining the location of this pin connection on the EVM.
3. If available, connect this fixed duty cycle signal to a dc voltage converter and use it to control the speed of a dc motor by varying the duty cycle of the waveform.
4. Modify the above program to now create a sinusoidally modulated PWM signal on the GP Timer Compare pin. To do this, a sinusoidal look-up

table can be created separately and then included with the source code. To modulate the signal, the timer compare register needs to be repeatedly updated with the modulation signal at a desired rate for a particular sinusoidal output frequency.

5. Write another program that creates the sinusoidal PWM, but instead uses the Compare Units.
6. If available, connect the two PWM outputs of the compare unit to a power inverter and run a single-phase induction motor. Vary the speed of the motor by manually varying the magnitude and rate at which the compare registers are updated with the modulation signal. Maintain a constant voltage/frequency (V/Hz) ratio to the induction motor.