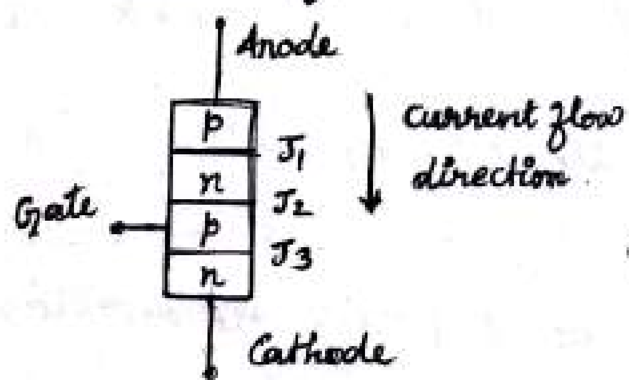
Structure, Operation and Characteristics of SCR

Thyristor is a 4-layered, 3-junction pnpn semiconductor switching device.

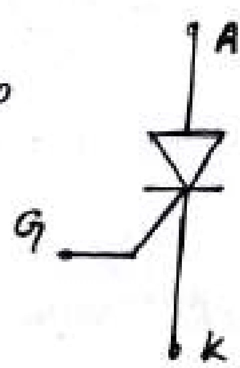
Has 3 terminals - Anode, Cathode and Gate.

SCR is an unidirectional device.

Schematic diagram



Circuit Symbol



The thyristor consists of four layers of alternate p-type & n-type silicon semiconductors forming three junctions J_1, J_2 & J_3.

The terminal connected to outer p-region forms anode 'A', the terminal connected to outer n region is called ~~gate~~ 'Cathode 'K'.

The Gate terminal is usually kept near cathode terminal.

SCR's are solid state devices, they are compact, possess high reliability and have low loss.

Power handling capability is more.

Operation.

The thyristor has 3 basic modes of operation

Reverse blocking mode

Forward blocking mode

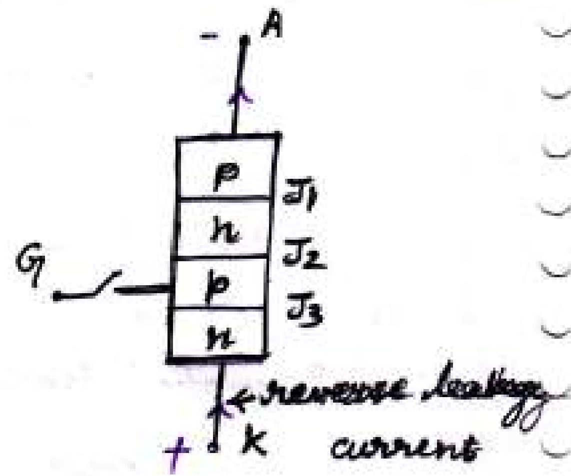
Forward conduction mode.

Reverse blocking mode.

The switch S open (i.e., gate open)

Cathode is made positive with respect to anode.

∴ The thyristor is reverse biased.



The junctions J_1, J_3 are reverse biased whereas junction J_2 is forward biased.

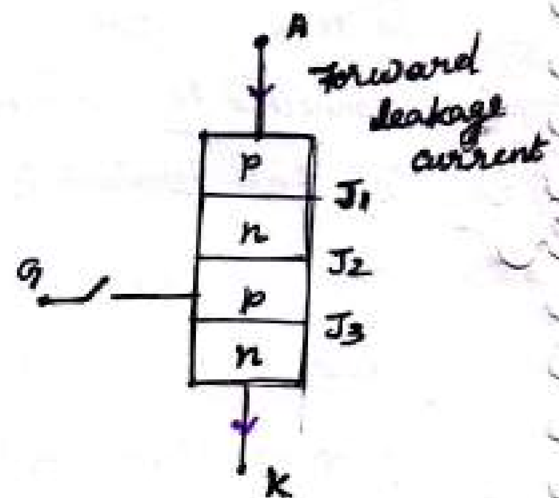
A small leakage current flows (of the order few mA or μA).

If the reverse voltage is ↑ed, then at reverse breakdown voltage V_{BR}, an avalanche occurs at J_1 & J_3 & the reverse current increases rapidly.

The large reverse current will lead to thyristor damage.

Forward blocking mode.

Here anode is positive with respect to cathode, with gate circuit open.



The thyristor is said to be forward biased.

Junctions J_1, J_3 are forward biased whereas junction J_2 is reverse biased.

In this mode, a small current, called forward leakage current flows.

As the forward leakage current is small, SCR offers a high impedance.

Therefore, a thyristor can be treated as an open switch even in the forward blocking mode.

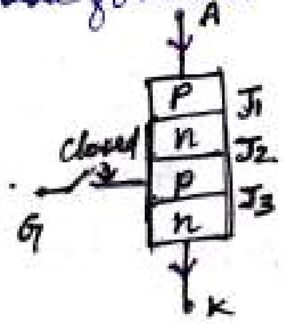
Foward Conduction mode.

A thyristor can be brought from forward blocking mode to forward conduction mode by applying

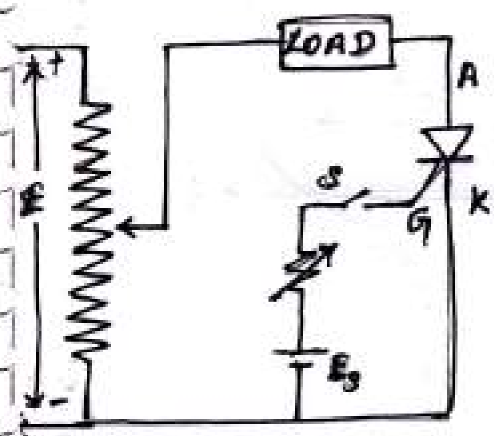
i) a positive gate pulse between gate & cathode. (Or)

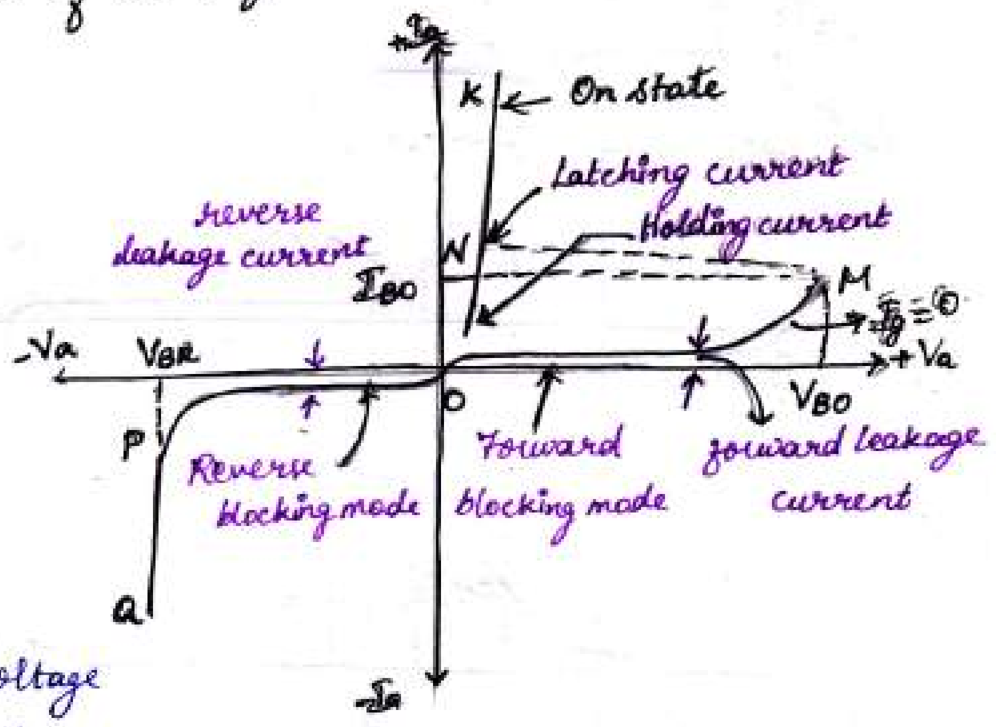
ii) by increasing the anode to cathode voltage above forward breakover voltage. (V_{BO})

After this breakdown, thyristor gets turned on.



I-V characteristics of a thyristor.





V_{BO} - Foward breakover voltage

V_{BR} - Reverse breakdown voltage.

I_g - Gate current.

V_a - Voltage across anode & cathode.

Latching current (I_L)

Minimum anode current required to bring the device into conduction.

Holding current (I_H)

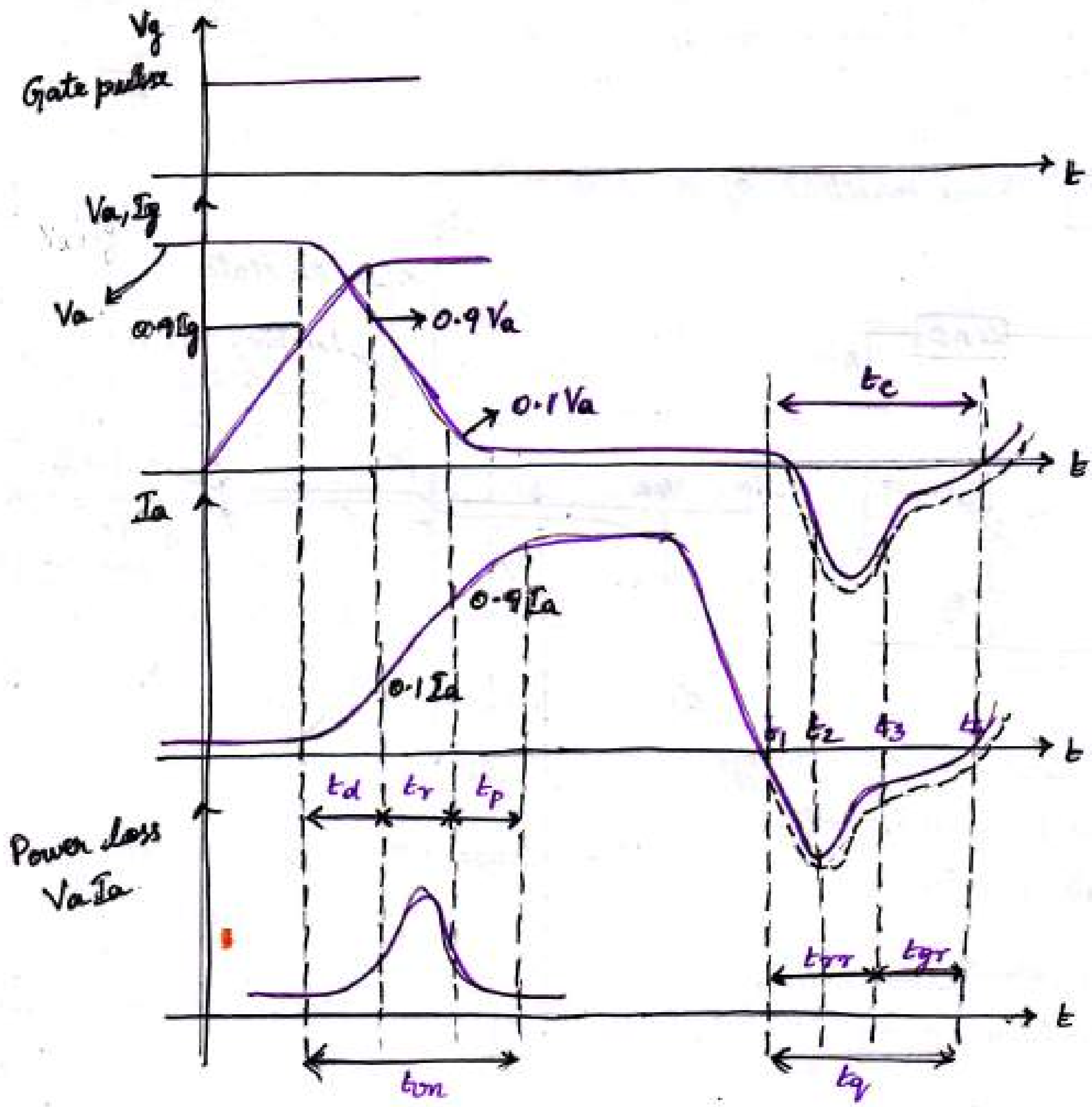
Minimum anode current required to maintain the device in 'ON' state.

I_L should always be higher than I_H ie, $I_L > I_H$.

Thyristor - turn ON methods

i) Forward voltage method
ii) Thermal triggering
iii) Radiation / Light triggering
iv) $\frac{dv}{dt}$ triggering
v) Gate pulse triggering
vi) Forward voltage triggering

Switching Characteristics of SCR



$t_{on} = t_d + t_r + t_p$

$t_q = t_{rr} + t_{gr}$

t_{on} - On time

t_q - off time

t_d - delay time

t_r - rise time

t_p - spread time

t_{rr} - reverse recovery time

t_{gr} - gate recovery time.

SCR is capable of being switched from fwd blocking state to fwd conduction state.

The transition from 1 state to the other does not take place instantaneously & it occupies the finite period of time. This period is known as transient period / transition time.

The variation of voltage & current during turn ON & OFF process gives the dynamic (or) switching characteristics.

SCR can be turn ON by applying +ve gate pulse b/w G & K.

Now the SCR switches from fwd blocking to fwd conduction state.

However, it takes some time for transition.

Turn-on time is divided into process
i) delay time (t_d)
ii) rise time (t_r)
iii) spread time (t_p)

Delay time (T_d)

It is measured from the instant at which gate current reaches I_g (90% of I_g) to the instant at which anode current reaches $0.1 I_a$.

It may also be defined as the time during which anode voltage falls from V_a to $0.9 V_a$.

$I_a \rightarrow$ Final value of anode current
$I_g \rightarrow$ " " " gate "
$V_a \rightarrow$ initial " " anode voltage.

The delay time can be red by applying high gate current & more forward voltage b/w anode & cathode.

Rise time (t_r)

It is the time taken by the anode current to rise from $0.1 I_a$ to $0.9 I_a$. (ie, 10% to 90% of I_a)

Also it can be defined as the time required for the forward blocking voltage to fall from $0.9 V_a$ to $0.1 V_a$.

Spread time (t_p)

It is the time taken by the anode current to rise from $0.9 I_a$ to I_a.

Also defined as time for the frwd blocking voltage to fall from $0.1 V_a$ to its frwd on state vol drop (1 to 1.5 volt)

Turn-off process

Thyristor turn off means that it has changed from on to off state & is capable of blocking frwd voltage.

This dynamic process of SCR from frwd conducting state to frwd blocking state is called commutation / turn-off process.

Once, the thyristor is ON, the gate losses its control.

The SCR can be turned off by reducing the anode current below holding current.

turn off time (t_q)

During time t_q, all the excess carriers from the 4 layers of SCR must be removed.

This removal of excess carriers consists of sweeping out of holes from outer P layer & electrons from N layer. The carriers around the junction (J_2) can be removed only by recombination.

Reverse recovery time (t_{rr})

At instant t_1, anode current becomes zero & after t_1, I_a builds in the reverse direction.

The reason for reversal of anode current is due to the presence of carriers stored in the four layers during conduction.

In order to turn-off the thyristors, these carriers should be removed.

Reverse recovery current removes carriers from junctions J_1 & J_3 between the instants T_1 & T_3.

At T_2, when about 60% of the stored charges are removed from the outer layers, & the t_{rr} ↓s & starts decaying.

Gate recovery time (t_{gr})

At T_3, the excess carriers in J_1 & J_3 are removed & they can block reverse voltage.

At the end of T_3, the middle junction J_2 still has some trapped charges.

The thyristor is unable to block the frwd vol.

These charges cannot flow through external circuit & can be removed only by recombination.

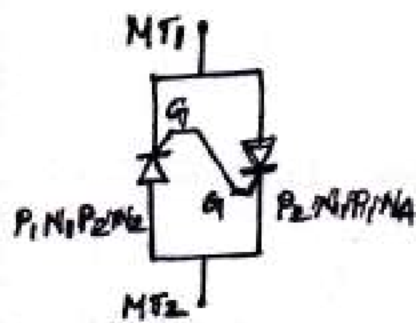
$$\therefore \boxed{T_q = t_{rr} + t_{gr}}$$

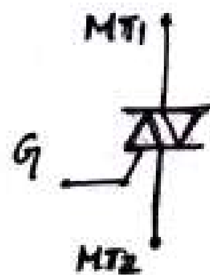
Structure, Operation & Characteristics of TRIAC

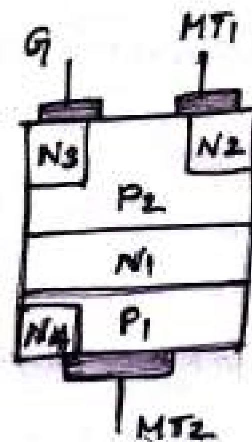
TRIode & AC.

Bidirection thyristor with three terminals (MT1, MT2 & G)

Two thyristors connected antiparallely (ie., back to back)







The triac can conduct in both the directions, the terms anode & cathode are not applicable to triac.

Its three terminals are represented as MT1 (Main terminal 1), MT2 (Main terminal 2) and the gate by G.

The Gate G is near terminal MT1 & it is connected to N3, P2 as well as ~~to~~.

Similarly, terminal MT1 is connected to P2 & N2; &

terminal MT2 is connected to P1 & N4.

Triac can be turned on in each half cycle of the applied voltage by applying a positive or negative voltage to the gate with respect to MT1.

It operates in 4 modes.

Forward blocking mode

Forward Conduction mode

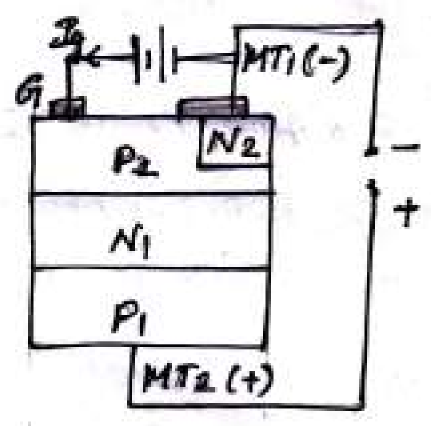
Reverse blocking mode

Reverse conduction mode.

Based on the biasing given to the terminals,

Mode 1:

MT_1 : -ve MT_2 : +ve G : +ve



$P_1 N_1$, $P_2 N_2$ → FB

$N_1 P_2$ → RB.

When G - +ve w.r to MT_1,

I_g flows through $P_2 N_2$ junction mainly.

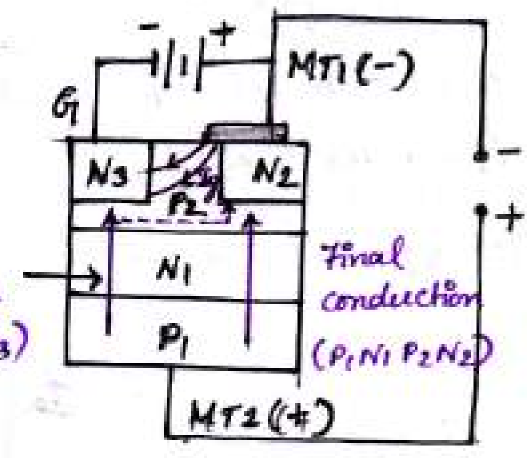
When I_g has injected sufficient charge in P_2 layer, RB junction $N_1 P_2$ breaks down ~~fast & therefore triac operates in I quadrant~~.

Triac now starts conducting through $P_1 N_1 P_2 N_2$ layers.

Under this condition, triac operates in I quadrant.

Mode 2:

MT_1 : +ve MT_2 : +ve G : -ve



When gate terminal is -ve w.r.to MT_1, I_g flows through $P_2 N_3$ junction.

$N_1 P_2$ - FB

∴ Initially, triac starts conducting through $P_1 N_1 P_2 N_3$ layers.

The voltage drop across this path falls but potential of layer b/w P_2 N_3 rises towards the anode potential of MT_2.

The potential gradient exists across P_2 [as right hand portion of P_2 is Clamped]

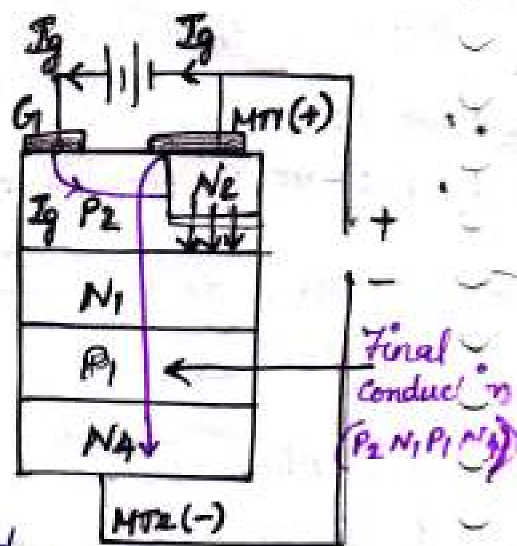
Left hand region of P_2 → higher potential

Right " " " " → Lower "

As a consequence, right hand part of triac consisting of $P_1 N_1 P_2 N_2$ begins to conduct.

Mode 3 :

MT_1 : +ve MT2 : -ve G : +ve



~~Ig flows~~ P_2 to N_2.

RB jn $N_1 P_1$ is broken.

Finally, $P_2 N_1 P_1 N_4$ is turned on completely.

$P_2 N_2$ - FB.

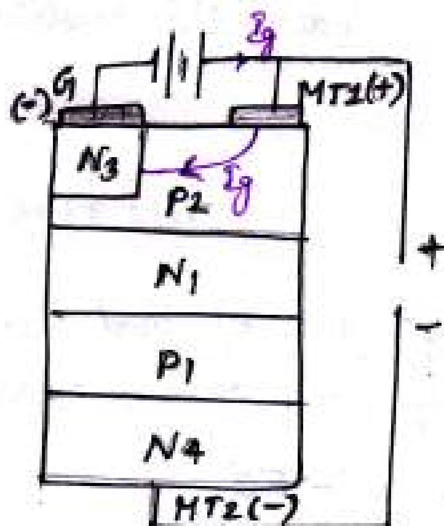
Layer N_2 injects e's into P_2 layer (dotted arrows).

As a result, RB jn $N_1 P_1$ breaks down.

Eventually, $P_2 N_1 P_1 N_4$ - on.

Mode 4 :

MT1 : +ve MT2 : -ve G : -ve

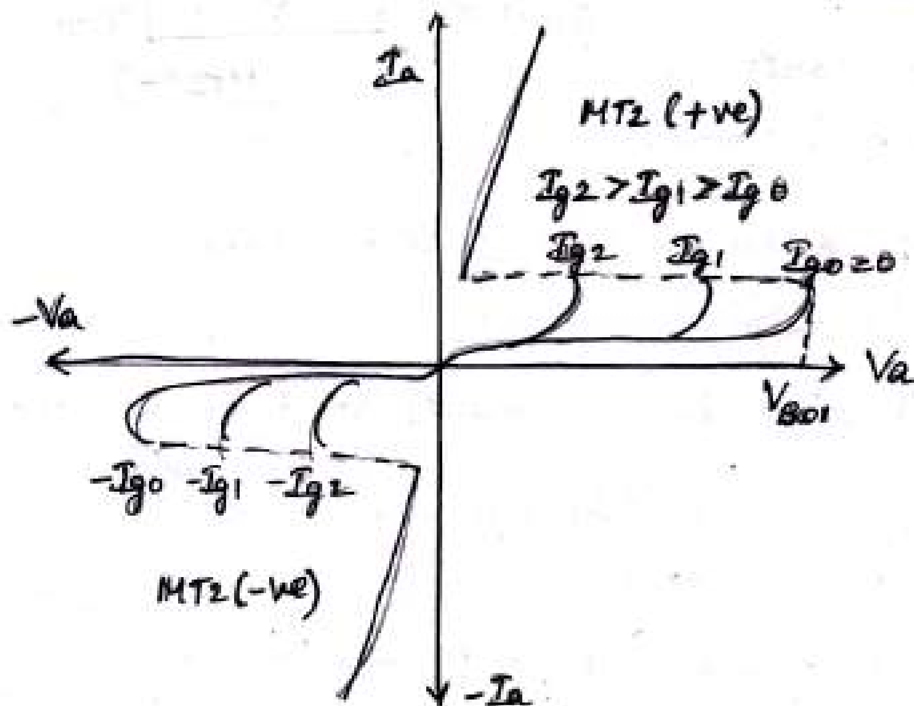


I_g flows from P_2 to N_3.

$N_1 P_1$ - broken & finally

$P_2 N_1 P_1 N_4$ - on.

Static VI Characteristics.

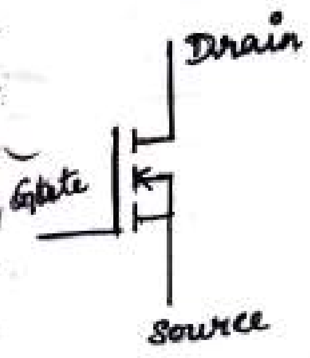


Power MOSFET's (Metal-oxide-semiconductor field-effect transistor)

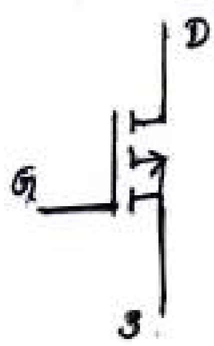
- Voltage controlled device.
- Unipolar device.
- Consists of 3 terminals drain(D), source (S) and gate (G).
- 2 types
  - n-channel enhancement MOSFET. (most commonly used)
  - p-channel enhancement MOSFET

Symbol

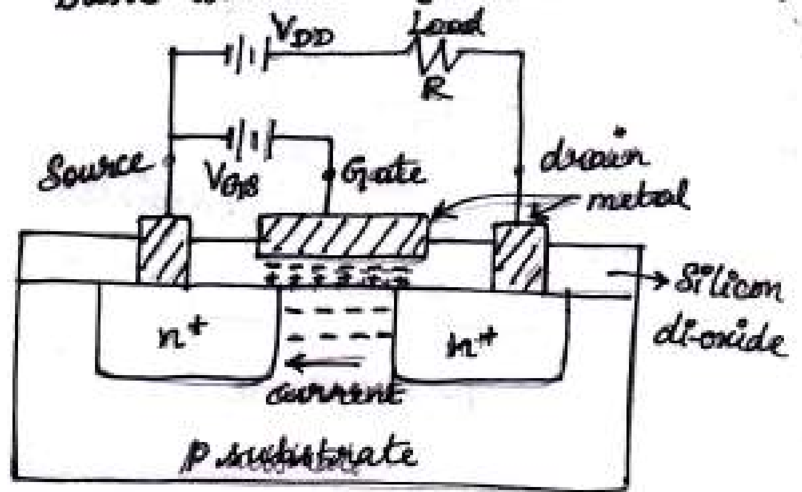
n-channel



p-channel



basic structure (n-channel MOSFET)



On p-substrate, two heavily doped n^+ regions are diffused.

An insulating layer of silicon dioxide (SiO_2) is grown on the surface.

This insulating layer is etched in order to embed metallic source and drain terminals.

A layer of metal is also deposited on SiO_2 layer so as to form the gate of MOSFET in between source & drain terminals.

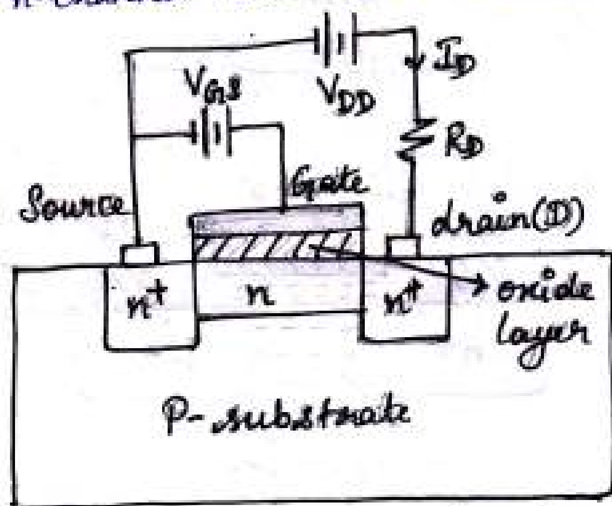
Power Mosfet's requires base current for current flow in the collector & also it requires only a small I/p current.

The switching speed is very high & the switching times are of the order of nanoseconds.

Power Mosfet's find applications in low power high frequency converters.

An n-channel enhancement-type Mosfet has no physical channel. When V_{GS} +ve, an induced voltage attracts the electrons from p-substrate & accumulate them at the surface beneath the oxide layer.

When V_{GS} is greater than or equal to a value known as threshold voltage V_T, a sufficient number of e^-s are accumulated to form a virtual n-channel and the current flows from the drain to source.



n-channel depletion type MOSFET

An n-channel depletion-type Mosfet is formed on a p-type silicon substrate.

The gate is isolated from the channel by a thin oxide layer.

The three terminals are called gate, drain & source.

The substrate is normally connected to the source.

The gate to source voltage V_{GS} could be either +ve or -ve.

If V_{GS} is negative, some of the e^-s in the n-channel are repelled & a depletion region is created below the oxide layer, resulting in a narrower effective channel & a high resistance from drain to source R_{DS}.

Therefore no current flows from drain to source, $I_{DS} = 0$.

The value of V_{GS} when this happens is called pinch-off voltage V_P.

Insulated Gate Bipolar Transistor (IGBT)

IGBT is a combination of both BJT and MOSFET.

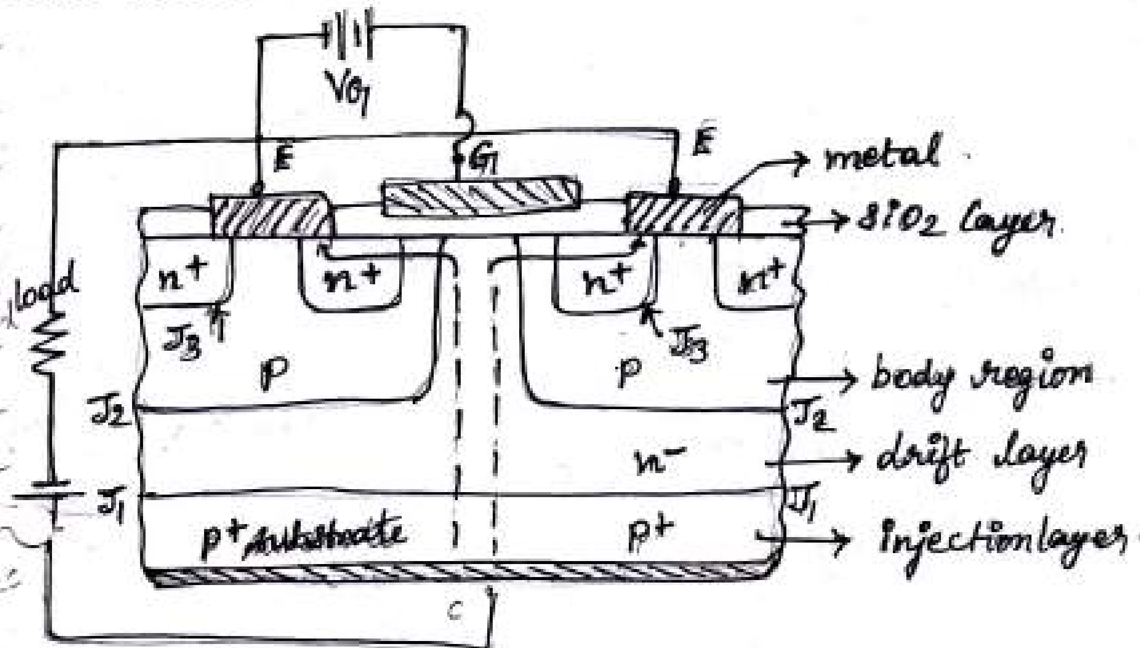
Thus IGBT possesses high input impedance like a power MOSFET and has low on-state power loss as in a BJT.

Further, IGBT is free from second breakdown problem present in BJT.

IGBT is also known as metal oxide insulated gate transistor (MOSIGT), conductively-modulated field effect transistor (COMFET) or gain-modulated FET (GEMFET).

Also called as insulated gate transistor (IGT).

Basic structure.



The construction of Mosfet is similar in structure as power Mosfet except a thing.

The major difference is that n^+ layer substrate at the drain in a Power Mosfet is substituted in the IGBT by a p^+ layer substrate called collector C.

In IGBT, p^+ substrate is called injection layer because it injects holes into n^- layer.

The n^- layer is called drift region.

The thickness of n^- layer determines the voltage blocking capability of IGBT.

The p layer is called body of IGBT.

The n^- layer in between p^+ & p regions serves to accomodate the depletion layer of pn^- junction (ie, J_2)

Working

When collector is made positive with respect to emitter, IGBT gets forward biased.

With no voltage between gate & emitter, two junctions between n^- region & p region (ie, J_2) are reverse biased; so no current flows from collector to emitter.

When gate is made positive w.r.to emitter by voltage V_{G}, with gate-emitter voltage more than the threshold voltage V_{GET} of IGBT, an n-channel or inversion layer, is formed in the upper part of p-region just beneath the gate, as in power Mosfet.

This n-channel short ckts the n^- region with n^+ emitter regions.

Electrons from n^+ emitter begin to flow to n^- drift region through n-channel.

As IGBT is frwd biased with collector positive & emitter negative, p^+ collector region injects holes into n^- drift region.

With this, the injection carrier density in n^- drift region is considerably & as a result, conductivity of n^- region enhances significantly.

Therefore, IGBT gets turned on & begins to conduct forward current I_C.

What is latchup in IGBT?

IGBT switching characteristics.

Turn-on time

It is defined as the time b/w the instants of forward blocking to forward on-state.

Turn-on time is composed of delay time (t_{dn}) and rise time (t_r).

ie, $t_{on} = t_{dn} + t_r$

Delay time (t_{dn})

It is defined as the time for the collector-emitter voltage to fall from V_{CE} to $0.9 V_{CE}$. $V_{CE} \rightarrow$ Initial collector-emitter vol.

It is also defined as the time for the collector current to rise from its initial leakage current I_{CE} to $0.1 I_C$.

$I_C \rightarrow$ final value of collector c/y.

Rise time (t_r)

It is the time during which collector-emitter voltage ~~volto~~ falls from $0.9 V_{CE}$ to $0.1 V_{CE}$.

It is also defined as the time for the collector current to rise from $0.1 I_C$ to its final value I_C.

After time t_{on}, the I_C & V_{CE} falls to small value called conduction drop = V_{CES} (here S denotes → saturated value)

Turn-off time

It consists of 3 intervals delay time (t_{df}), initial fall time (t_{f1}) and final fall time, (t_{f2}).

ie, $t_{off} = t_{df} + t_{f1} + t_{f2}$

Delay time (t_{df})

It is the time during which gate voltage falls from V_{GE} to threshold voltage V_{GET}.

As V_{GE} falls to V_{GET} during t_{df}, the collector current falls from I_C to $0.9 I_C$.

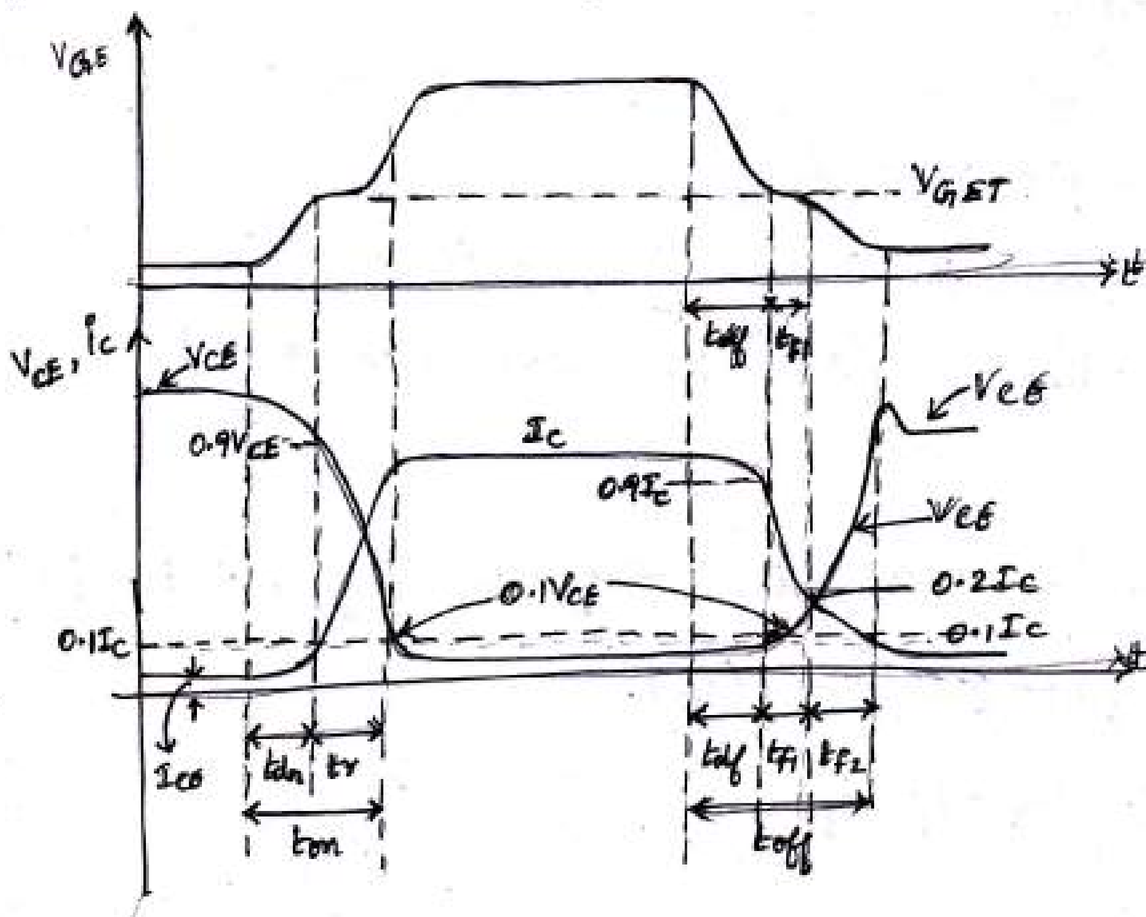
At the end of t_{df}, collector-emitter voltage begins to rise.

First fall time (t_{f1})

- defined as the time during which I_C falls from 90 to 20% of its value I_C.
- also defined as the time during which V_{CE} rises from V_{CES} to $0.1 V_{CE}$.

Final fall time (t_{f2})

- defined as the time during which I_C falls from 20 to 10% of I_C
- also defined as the time during which V_{CE} rises from $0.1 V_{CE}$ to final value V_{CE}.



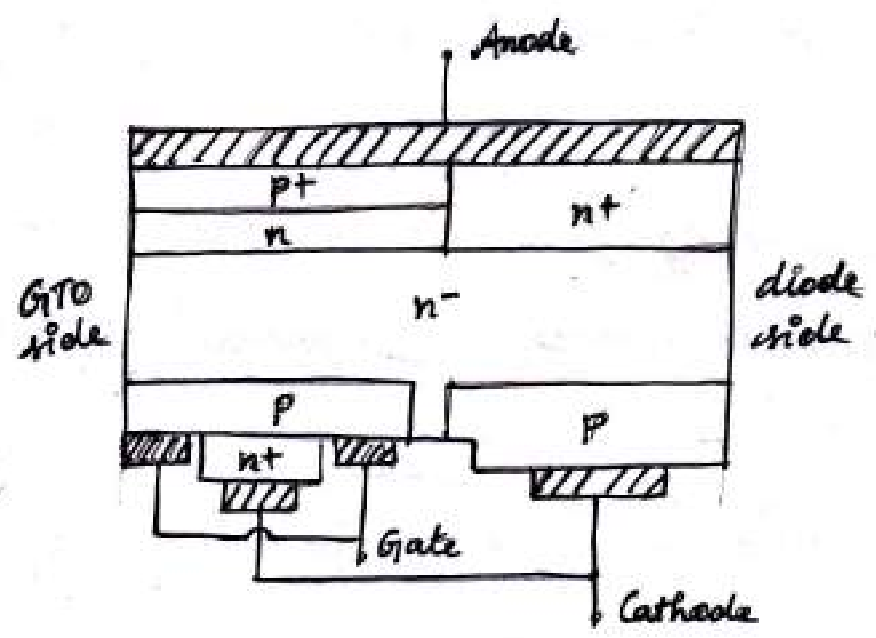
IGCT (Integrated Gate Commutated Thyristor)

The IGCT integrates a gate-commutated thyristor (GCT) with a multilayered printed circuit board gate drive.

The GTO is a hard-switched GTO with a very fast and large gate current pulse, as large as the full rated current, that draws out all the current from the cathode into the gate in about 1 μs to ensure a fast turn-off.

The internal structure & equivalent circuit of a GCT are similar to that of a GTO.

Cross section of IGCT with a reverse diode



An IGCT may also have an integrated reverse diode, as shown by the $n^+ n^- p$ junction on the right side of the IGCT structure.

Similar to a GTO, an MTO (MOS turn-off thyristors) & an ETO (Emitter turn-off thyristors), the n^- buffer layer evens out the voltage stress across the n^- layer, reduces the thickness of n^- layer, the on-state conduction losses, & makes the device asymmetric.

The anode p-layer is made thin & lightly doped to allow faster removal of charges from the anode-side during turn-off

Turn-on

Similar to GTO, the IGCT is turned on by applying the turn-on current to its gate.

Turn-off

The IGCT is turned off by a multilayered gate driver ckt board that can supply a fast rising turn-off pulse.

Due to a very-short duration pulse, the gate-drive energy is greatly reduced and the gate-drive energy consumption is minimized.

The gate-drive power requirement is red by a factor of five compared with that of the GTO.

To apply a fast-rising & high-gate current, the IGCT incorporates a special effort to reduce the inductance of the gate circuitry as low as possible.

This feature is also necessary for gate-drive circuits of the MTO & ETO.

Refer Rashid.

Adv of GTOs over SCR & BJT

Gate turn off thyristor (GTO)

Conventional thyristors (CTs) can be easily turned on by +ve gate cty.

The gate loses its control once it comes to on-state.

The CTs can now be turned off by expensive & bulky commutation circuity.

These drawbacks had led to the development of GTOs.

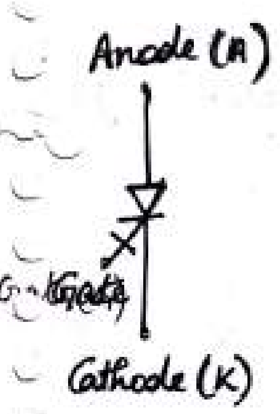
A GTO like an SCR can be turned on by applying +ve gate signal.

However, a GTO can be turned off by a -ve gate signal.

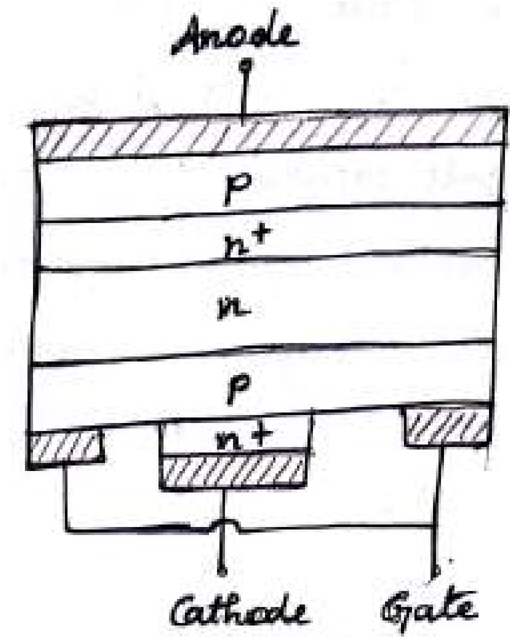
A GTO is a non-latching device & can be built with cty & vol ratings similar to those of an SCR.

A GTO can be turned on by applying a short +ve pulse & turned off by a short -ve pulse to its gate.

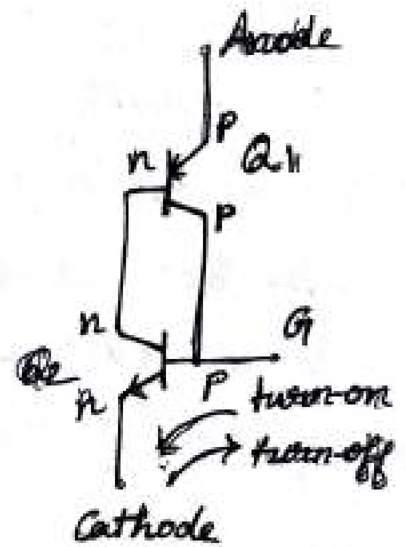
It is a latch-on device, but it is also a latch off device.



(a) Symbol



(b) Cross section



(c) Equivalent circuit

A GTO is pnpn, three terminal device with anode (A), cathode (K) & gate (G).

Compared to a CT, it has an additional n^+ layer near the anode that forms a turnoff ckt b/w the G & K in ||el with the turn-on gate.

Turn-on

The GTO has a highly interdigited gate structure with no regenerative gate.

As a consequence, a large initial gate trigger pulse is required to turn on.

Once the GTO is turned on, forward gate current must be continued for the whole of the conduction period to ensure the device remains in conduction.

Otherwise, the device cannot remain in conduction during the on-state period.

The on-state gate ct should be atleast 1% of the turn-on pulse to ensure that the gate doesnot latch.

Turn-off

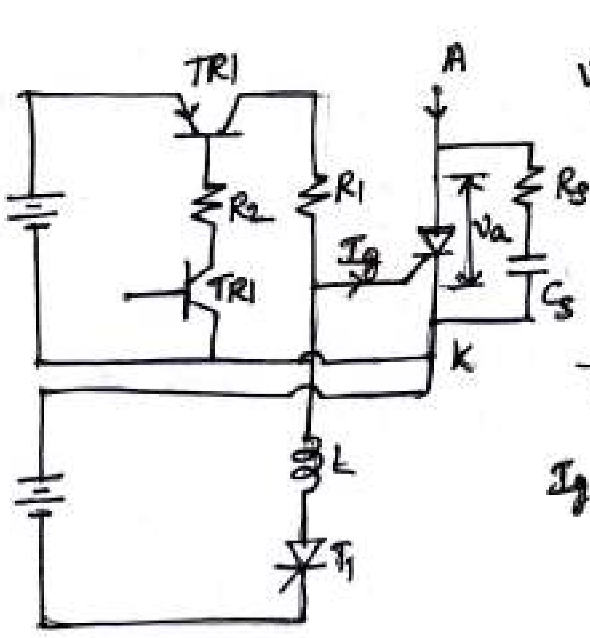
The turn-off process is quite diff from that in a CT.

For initiating the turn-off process in a GTO, a negative gate current is applied across gate-cathode terminals.

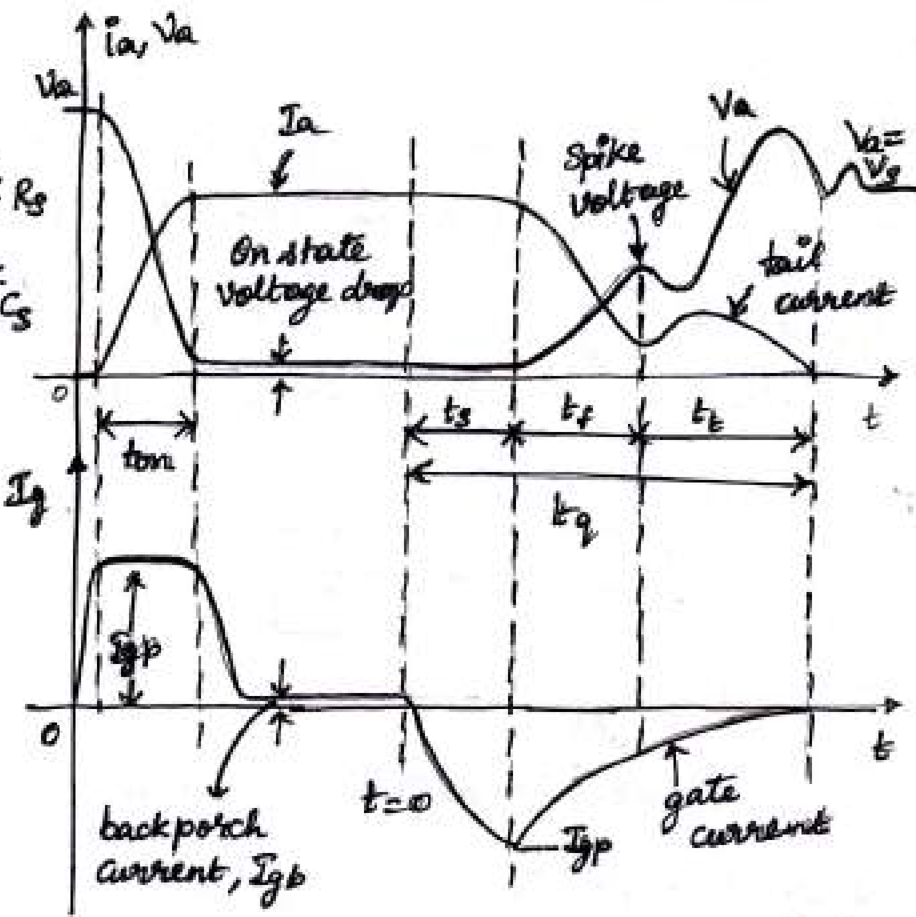
Also Q2 must be brought out of saturation.

So, Q2 would shift to active region & regenerative action would eventually turn-off the GTO.

Switching characteristics of GTO.



a) Basic drive circuit



For turning-on a GTO, first transistor TR1 is turned on, this in turn switches on TR2 to apply a +ve gate-ct pulse to turn-on GTO.

For turning off the GTO, the turn-off ckt should be capable of outputting a high peak ct.

The turn-off process is initiated by gating thyristor T_1.

When T_1 is on, a large -ve gate current pulse turns off the GTO.

Gate turn-on

The gate turn-on time of GTO is made up of delay time, rise time, and spread time like a CT.

Further, turn-on time in a GTO can be ↓ed by ↑ing its forward gate current as in a thyristor.

A steep-fronted gate pulse is applied to turn-on GTO.

~~Gate turn-on time for VG~~

Gate drive can be removed once anode c/y exceeds latching current.

However, some manufacturers advice that even after GTO is on, a continuous gate c/y, called back porch c/y I_{gb} should be applied during the entire on-period of GTO.

This is done to avoid any possibility of unwanted turn-off of the GTO.

$$T_{on} = t_d + t_r + t_p$$

Gate turn-off

Before the initiation of turn-off process, a GTO carries a steady current I_a.

The total turn-off time t_q is subdivided into three diff periods; namely the storage period (t_s), the fall period (t_f) and the tail period (t_t).

$$t_q = t_s + t_f + t_t$$

Storage time (t_s)

When the -ve gate current is applied, the turn off process is initiated.

During the storage period, anode c/y I_a & anode voltage remain constant.

Termination of the storage period is indicated by a fall in I_a & rise in V_a.

During t_s, the -ve gate c/y rises to a particular value & prepares the GTO for turn-off by flushing out the stored carriers.

After t_s, I_a falls to a certain value & then abruptly changes its rate of fall.

Fall time (t_f)

The interval during which I_a falls rapidly is called t_f & is of the order of 1 µsec.

At $= t_s + t_f$ At the time $t = t_s + t_f$, there is a spike in voltage due to abrupt change in anode ckt.

Tail time (t_t)

After t_f, I_a & V_a keep moving towards their turn-off values for a time t_t (tail time).

After t_t, I_a reaches zero value & V_a undergoes a transient overshoot due to the presence of R_s, C_s & then stabilizes to its off-state value equal to the source voltage applied to the anode ckt.

Here R_s & C_s are the snubber circuit parameters.

The turn-off process is complete when tail ckt reaches zero.

Application of GTO's

Power transistor - BJT

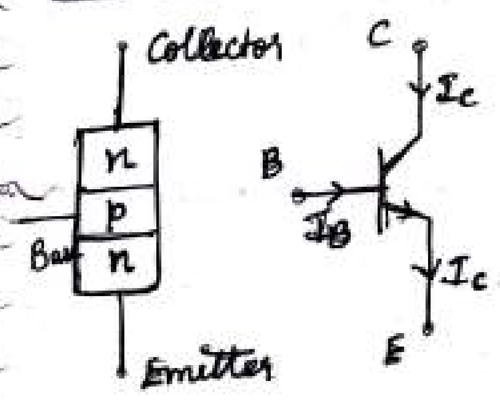
A bipolar transistor is a 3 layer, 2 jn npn (or) pnp semiconductor device.

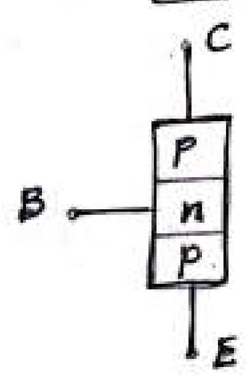
With one p-region sandwiched by two n-regions → npn transistor.

With one n-region " " " p " → pnp "

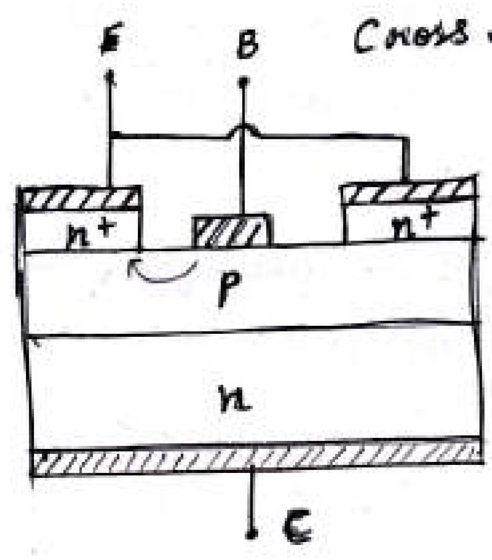
A BJT has 3 terminals named collector (C), emitter (E) & base (B).

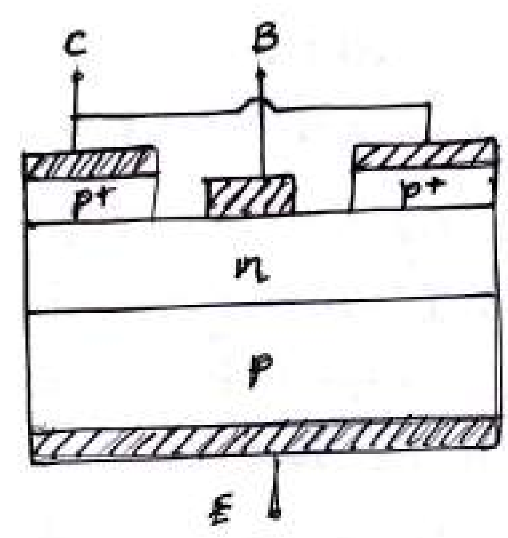
npn - transistor Symbol pnp - transistor





Cross section





For an NPN-type, the emitter side n-layer is made wide, the p-base is narrow, and the collector side n-layer is narrow and heavily doped.

For a PNP-type, the emitter side p-layer is made wide, the n-base is narrow, & the collector side p-layer is narrow & heavily doped.

The base & collector currents flow through two parallel path resulting in a low on-state collector-emitter resistance, R_{CE} (ON).

Power transistors of npn type are easy to manufacture & are cheaper also.

Therefore, use of power n-p-n transistors is very wide in high voltage & high-current applications.

There are 3 possible ckt configurations for a transistor, CE, CC, & CB. Out of this, CE configuration is more common in switching applications.

There are 3 operating regions of a transistor: cut off, active & saturation.

Cutoff region

In this region, the transistor is off or the base current is not enough to turn it on & both junctions are reverse biased.

Active region

In this region, the transistor acts as an amplifier, where the base current is amplified by a gain & the collector-emitter voltage ↓s with the base ct.

The collector-base jn is RB (Reverse Bias) & base-emitter jn is FB.

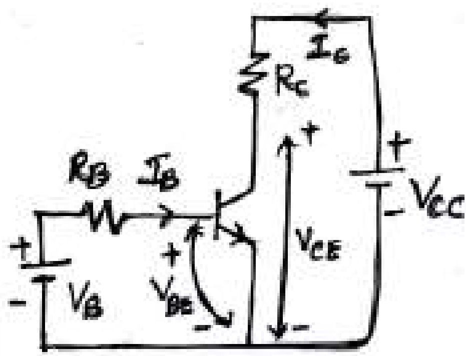
In this region, the transistor like an amplifier.

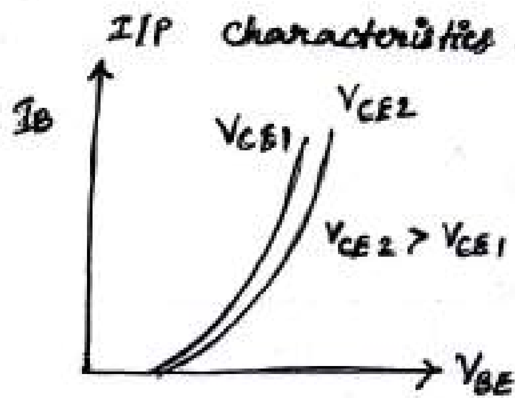
Saturation region.

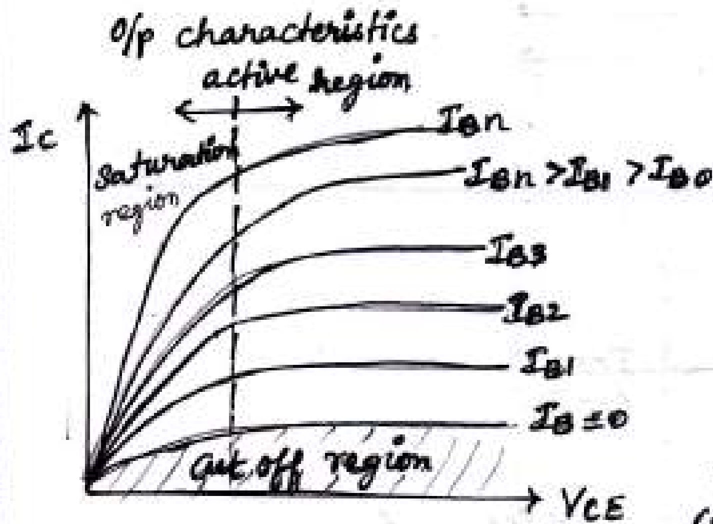
The base ct is sufficiently high so that the collector-emitter voltage is low & the transistor acts as a switch.

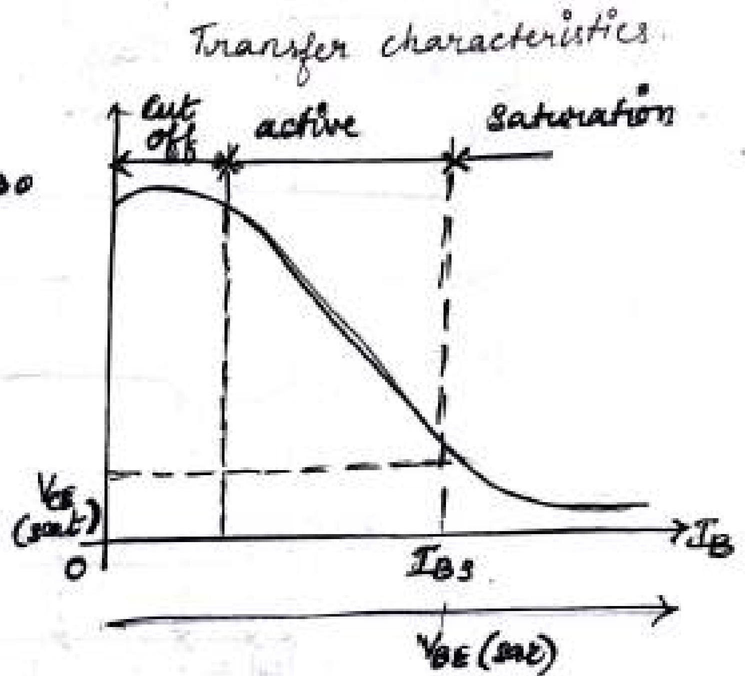
Both jn's (C·B jn & B·E jn) are frwd biased.

In this region, the transistor acts like a switch.









Current gain $\beta = \frac{I_C}{I_B}$

Forward current gain $\alpha = \frac{I_C}{I_E}$

Relation between α & β $\qquad \alpha = \frac{\beta}{\beta+1}$

$I_E = I_C + I_B$ $\qquad \beta = \frac{\alpha}{1-\alpha}$

÷ both by I_C

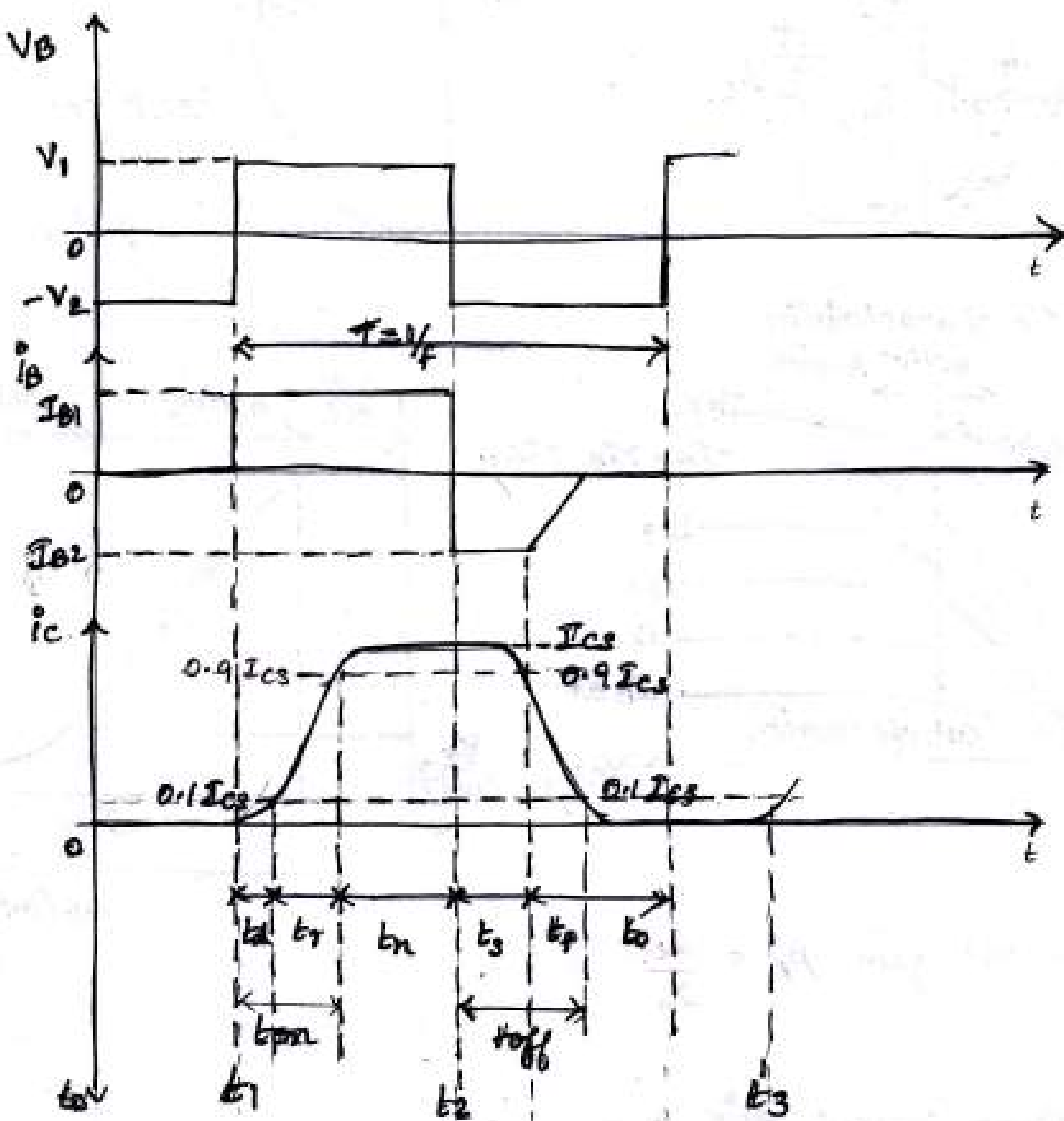
transis as switch → cutoff & sat.

cutoff $\quad I_C = 0 \quad P_L = V_{CE} \times I_C = V \times 0 = 0$

sat $\quad V_{CE} = 0 \quad P_L = V_{CE} \times I_C = 0 \times I_C = 0$

$$I_B = \frac{V_B - V_{BE}}{R_B} \; ; \; I_C = \frac{V_{CC} - V_{CE}}{R_C}.$$

Switching Characteristics of power BJT



When base current is applied, a transistor doesnot turn on instantly b/o of the presence of internal capacitances.

When i/p voltage V_B to base ckt is made $-V_2$ at t_0, the EB jn is RBiased, $V_{BE} = -V_2$, the transistor is off, $i_B = I_C = 0$ & $V_{CE} = V_{CC}$.

At t_1, i/p vol V_B is made $+V_1$ & i_B rises to I_{B1}.

After t_1, V_{BE} begins to rise from $-V_2$ & i_C begins to rise from 0 & V_{CE} starts ↓ing.

After some time delay t_d, called delay time, the i_c rises to $0.1 I_{CS}$, V_{CE} falls from V_{CC} to $0.9 V_{CC}$.

This delay time is required to charge the base-emitter capacitance to $V_{BES} = 0.7V$.

Thus delay time (t_d) is defined as the time during which the i_c rises from 0 to $0.1 I_{CS}$ & V_{CE} falls from V_{CC} to $0.9V_{CC}$.

After t_d, I_C rises from $0.1 I_{CS}$ to $0.9 I_{CS}$ & V_{CE} falls from $0.9 V_{CC}$ to $0.1 V_{CC}$ in time t_r.

The rise time t_r is defined as the time during which I_C rises from $0.1 I_{CS}$ to $0.9 V_{CC}$ & V_{CE} falls from $0.9 V_{CC}$ to $0.1 V_{CC}$.

t_r depends upon transistor jn capacitances.

Thus total turn on time $\boxed{t_{on} = t_d + t_r}$

At time t_2, i/p vol v_B to base ckt is reversed from V_1 to $-V_2$.

At the same time, base current changes from I_{B1} to $-I_{B2}$.

Negative base ct I_{B2} removes excess carriers from the base.

The time t_s required to remove these excess carriers is called storage time (t_s) & only after t_s, I_{B2} begins to ↓ to zero.

t_s is defined as the time during which I_C falls from I_{CS} to $0.9 I_{CS}$ & V_{CE} rises from V_{CES} to $0.1 V_{CC}$.

Fall time (t_f) is defined as the time during which I_C drops from $0.9 I_{CS}$ to $0.1 I_{CS}$ & V_{CE} rises from $0.1 V_{CC}$ to $0.9 V_{CC}$.

Thus $t_{off} = t_s + t_f$.

Gate triggering Circuit.

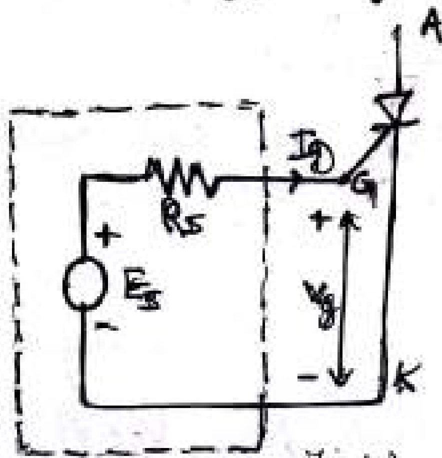


Fig (a)

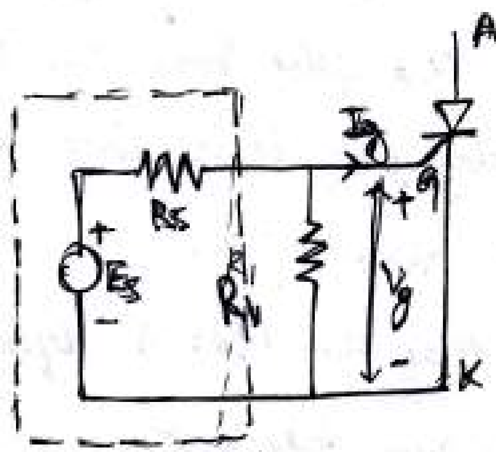


Fig (b)

Fig (a)

This is a trigger ckt feeding power to gate-cathode ckt.

For this ckt, $E_s = V_g + I_g R_s$.

E_s - gate source voltage. I_g - gate ct.

V_g - gate-cathode voltage R_s - gate-source resistance.

The internal resistance R_s of trigger source should be such that ct (E_s/R_s) is not harmful to the source as well as to the gate ckt when SCR is turned on.

In case R_s is low, an external resis in series with R_s must be connected.

A resistance R_1 is also connected across gate-cathode terminals in fig (b), so as to provide an easy path to the flow of leakage ct b/w SCR terminals.

If I_{gmn} & V_{gmn} are the min gate ct & gate vol to turn-on SCR, then it is seen from fig (b) that ct through R_1 is V_{gmn}/R_1 & the trigger source voltage E_s is given by

$$E_s = \left(I_{gmn} + \frac{V_{gmn}}{R_1} \right) R_s + V_{gmn}$$

For low-power ckts, it is customary to obtain the operating pt by utilizing the VI characteristics of both source & the device.

In view of this, for selecting the operating pt for the ckt fig a & b, a load line of the gate source voltage $E_s = OA$ is drawn as AD in fig C.

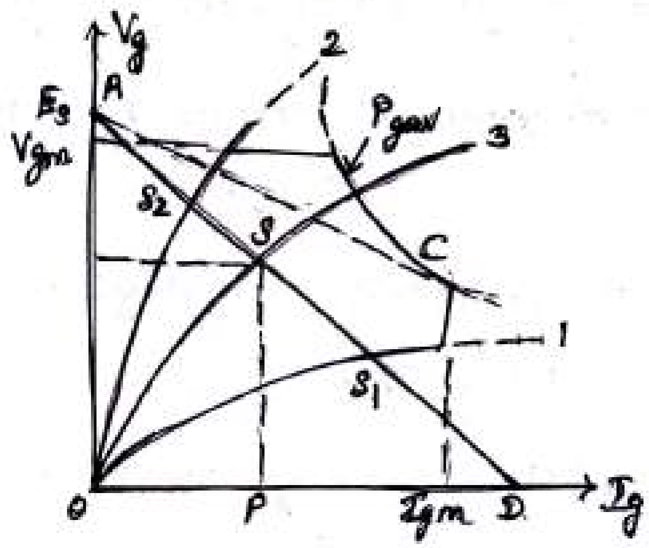


Fig C

Here OD = trigger ckt short circuit ct = E_s / R_s.

Let us consider a thyristor whose $V_g - I_g$ characteristic is given by curve 3.

Intersection of load line AD & $V_g - I_g$ curve 3 gives the operating pt S.

Thus for SCR, gate vol = PS & gate ct = OP.

In order to minimise turn-on time & unreliable turn-on, the load line & hence the operating pt S, which may change from S_1 to S_2, must be as close to the P_{gav} curve as possible.

At the same time, the operating pt S must lie within the limit curves 1 & 2.

The gradient of the load line AD (= OA/OD) will give the required gate source resistance R_s.

The minimum value of gate source series resistance is obtained by drawing a line AC tangent to P_{gav} curve.

Gate drive requirements in terms of continuous dc signal can be obtained from fig b.

However, it is common to use a pulse to trigger a thyristor.

Thyristor is considered to be a charge controlled device.

Thus, higher the magnitude of gate c/t pulse, lesser is the time to inject the required charge for turning-on the thyristor.

Therefore, SCR turn-on time can be reduced by using gate c/t of higher magnitude.

It should be ensured that pulse width is sufficient to allow the anode c/t to exceed latching c/t.

In practice, gate pulse width is usually taken as equal to or greater than, SCR turn-on time.

With pulse triggering, greater amount of power dissipation can be allowed; this should, however, be less than the peak instantaneous gate power dissipation P_{gm}.

Frequency of firing for trigger pulses can be obtained by taking pulse of (i) amplitude P_{gm} (ii) pulse width T & (iii) periodicity T_1.

$$\therefore \frac{P_{gm} T}{T_1} \geq P_{gav} \quad \text{or} \quad P_{gm} \cdot T \cdot f \geq P_{gav} \quad \text{or} \quad \frac{P_{gav}}{fT} \leq P_{gm} \rightarrow (1)$$

$f \rightarrow \frac{1}{T_1}$ = freq of firing (Hz) $\quad T$ = pulse width in sec.

In the limiting case, $\frac{P_{gav}}{fT} = P_{gm}$ or $f = \frac{P_{gav}}{T \cdot P_{gm}}$

Pulsed Gate drive

Instead of applying a continuous (DC) gate drive, the pulsed gate drive is used.

The gate vol & ch are applied in the form of high freq pulses.

The freq of these pulses is upto 10 kHz.

Hence the width of the pulse can be upto 100 μsec.

The pulsed gate drive is applied for following reasons.

i) The SCR has small turn-on time (ie, upto 5 μsec)
Hence a pulse of gate drive is sufficient to turn on the SCR.

ii) Once SCR turns-on, there is no need of gate drive.
Hence gate drive in the form of pulses is suitable.

iii) The DC gate vol & ch ↑s losses in the SCR. Pulsed gate drive has reduced losses.

iv) The pulsed gate drive can be easily passed through isolation transformers to isolate SCR & trigger ckt.

Requirement of Gate drive.

i) The max gate power should not be exceeded by gate drive, else SCR will be damaged.

ii) The gate vol & ch should be within the limits specified by gate charac for successful turn-on.

iii) The gate drive should be preferably pulsed.

iv) The width of the pulse should be sufficient to turn-on SCR successfully

v) The gate drive should be isolated electrically from the SCR.
This avoids any damage to the trigger ckt if in case SCR is damaged

vi) The gate drive should exceed permissible -ve gate to cathode vol, otherwise SCR is damaged.

vii) The gate drive ckt should not sink ch out of the SCR after turn-on.

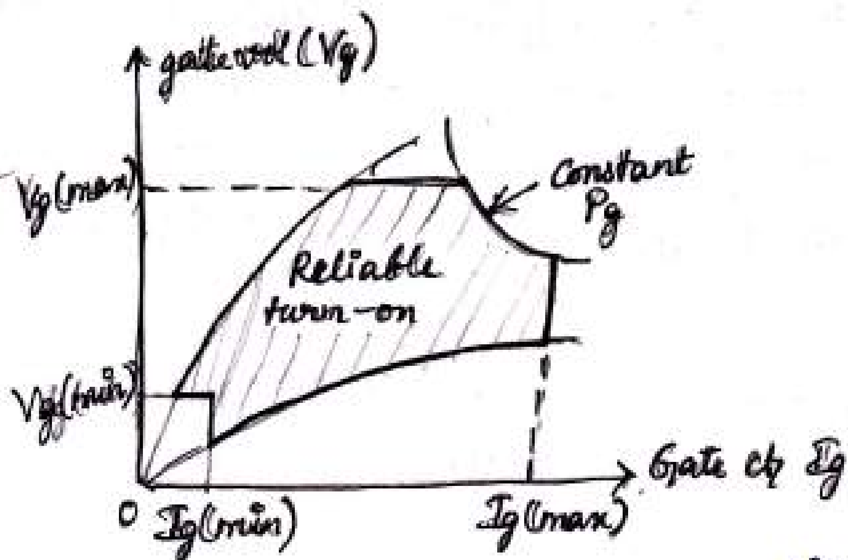
Inverter grade SCRs

The SCRs which have turn-off time less than 25 μs are called Inverter grade SCRs. Such SCRs are used in inverters, choppers etc.,

Converter grade SCRs

The SCRs having larger turn-off times ($t_q > 25\,\mu s$) are called converter grade SCRs. Such SCRs are used in controlled rectifiers, AC voltage ctlrs etc.,

SCR Gate characteristics.



The gate vol (V_g) is plotted w.r.to gate ct (I_g) in the charac.

$I_g(max) \rightarrow$ Max gate ct that can flow through SCR without damaging it.

$V_g(max) \rightarrow$ Max gate vol to be applied

$V_g(min)$ & $I_g(min) \rightarrow$ Min gate vol & ct, below which gate ct & vol should be

$$I_g(min) < I_g < I_g(max) \;\&$$

$$V_g(min) < V_g < V_g(max)$$

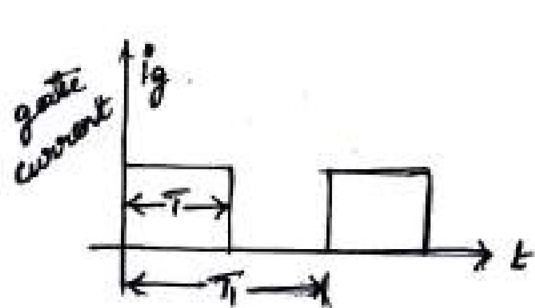
This is the curve for constant gate power (P_g).

Thus for reliable turn-on, the (V_g, i_g) pt must lie in the shaded area. It turns-on SCR successfully.

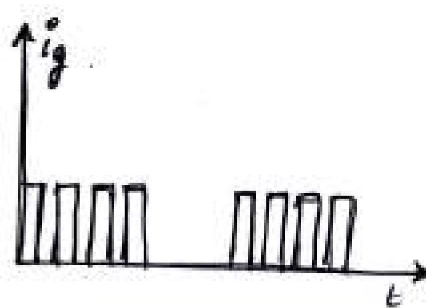
Note that any spurious vol/ct spikes at the gate must be less than $V_g(min)$ & $I_g(min)$ to avoid false triggering of SCR.

The gate shown here are for DC values of gate vol & ct.

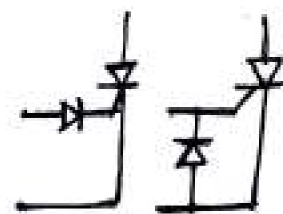
A duty cycle is defined as the ratio of pulse-on period to periodic time of pulse.



(d) Pulse gating



(e) high-frequency carrier gating of SCRs



(f) thyristor protection against reverse voltages.

In fig (d), pulse-on period is T & periodic time is T_1.

Therefore, duty cycle δ is given by, $\delta = \frac{T}{T_1} = fT$.

From ①, $\frac{P_{gav}}{\delta} \leq P_{gm}$ or $\frac{P_{gav}}{\delta} = P_{gm}$

Sometimes, the pulses of fig (d) are modulated to generate a train of pulses as shown in fig (e).

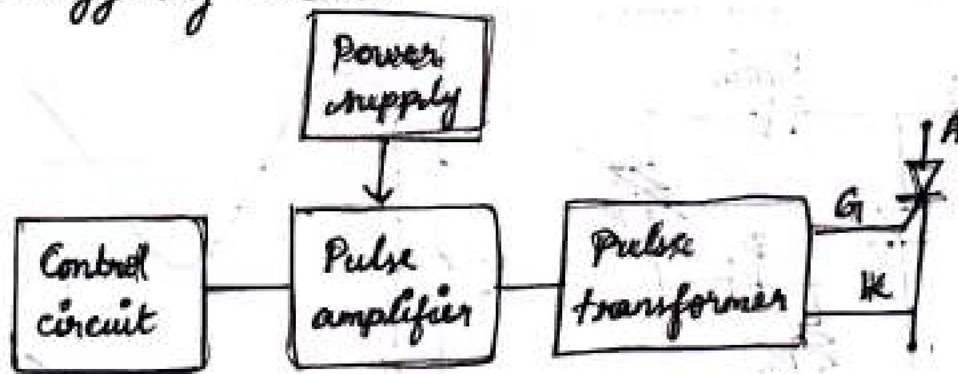
This technique of firing the thyristor is called high-frequency carrier gating.

The advantages offered by this method of firing the SCRs are lower rating, reduced dimensions & therefore an overall economical design of the pulse transformer needed for isolating the low power ckt from the main power ckt.

For an SCR, V_{gm} & I_{gm} are specified separately.

The magnitude of gate vol & gate ch for triggering an SCR is inversely proportional to jn temp.

Gate triggering Circuits



The firing ckt should produce the triggering pulses for every thyristor at appropriate instants.

The triggering pulses generated by ctrl ckt need to be amplified & passed through the isolation ckt.

The triggering pulses generated by ctrl ckt have very small power.

Hence their power is fed by pulse amplifier.

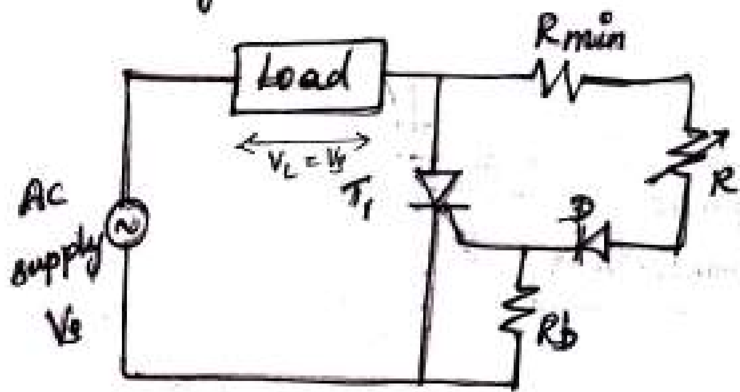
The firing ckt operates at low vol levels (5 to 20 volts).

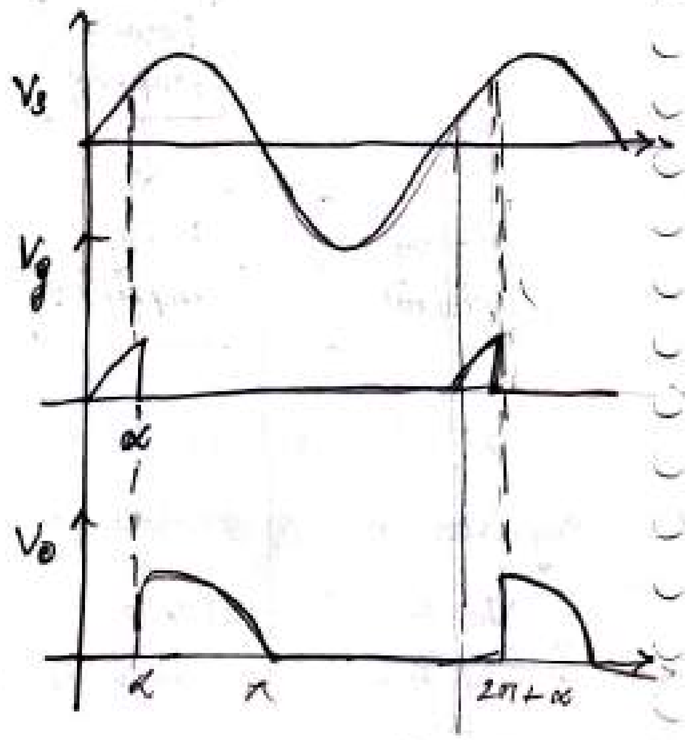
And the thyris operates at high vol levels (> 150 volts).

Hence there must be electrical isolation b/w firing ckt & thyristor.

This is provided by the pulse transformer or opto couplers.

R - Firing ckt.





R_{min} → used to limit I_g to its max value.

$$R_{min} \geq \frac{V_m}{I_g(max)}$$ V_m → peak supply vol.

R_b → stabilizing resis.
This should not exceed $V_g(min)$, else thyris will turn-on directly.

R → variable resis → to trigger T_1.
If R = 0, the triggering angle is min. R ↑s, angle ↑s.

The V_{AK} & I_g are inphase.
Hence the triggering angle of T_1 cannot be delayed beyond 90°.

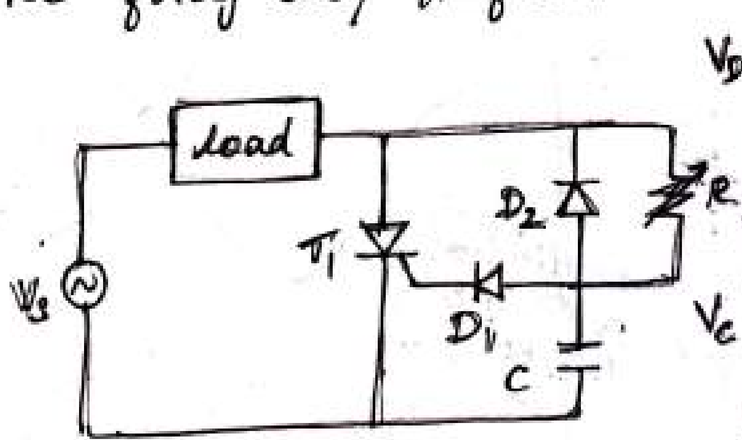
+ve half cycle → T_1 FB but will not conduct.
D_1 also FB. ∴ ct flowing through it will make T_1 to ON.
$V_L = V_s$.

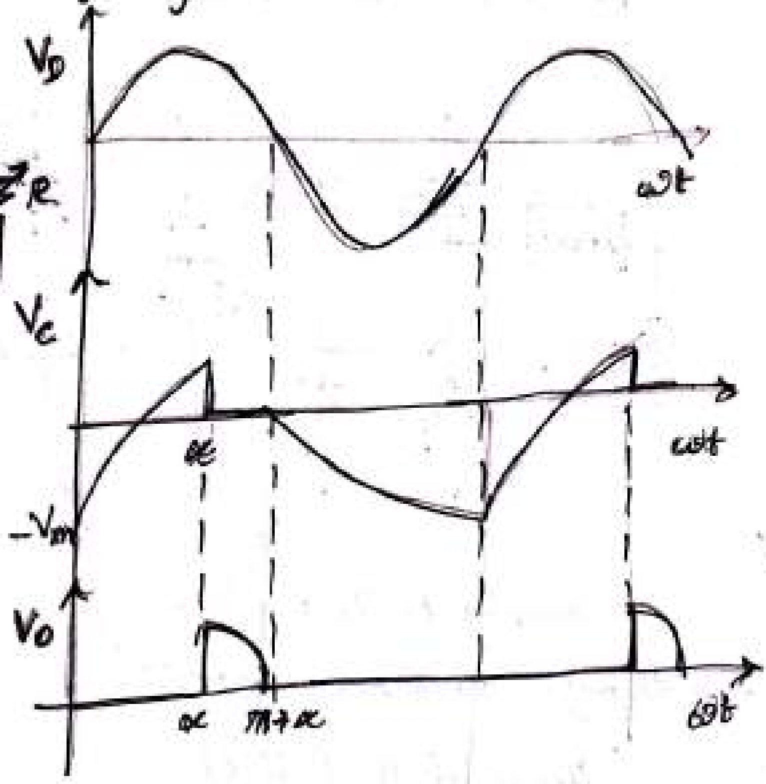
Disadv

α greatly dependent on SCR's I_g(min).
highly temp dependent.
Also α can be varied only up to 90° (0 to 90° only can be varied)

During -ve half cycle → Anode to Cathode of T_1 will be RB.
∴ T_1 - off.

RC firing ckt / Half wave RC firing ckt.





i) -ve half cycle

Cap 'C' charges to $-V_m$ through D_2 to -ve supply vol.

ii) +ve half cycle

'C' discharges (ie, charges towards +ve) through R during the +ve half cycle of the supply.

The thyris T_1 triggers when 'C' charges to value > V_g(min).

D_1 → prevents -ve capacitor vol appearing to gate of T_1.

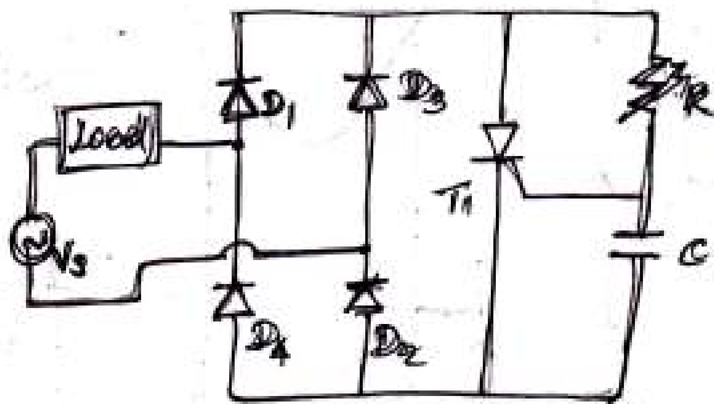
α → can be varied from 0 to 180°.

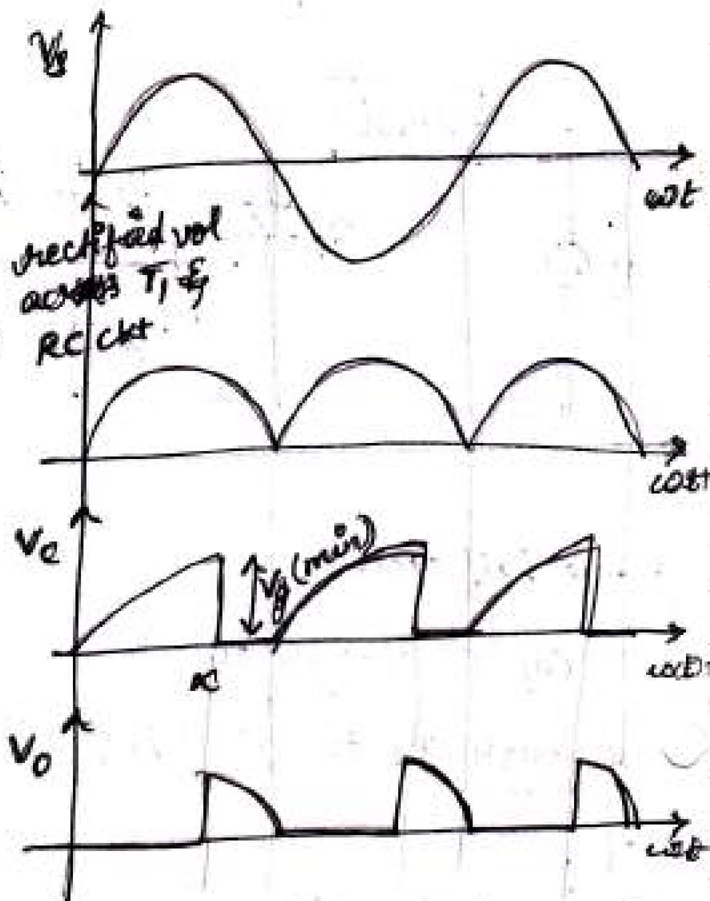
$$RC \geq \frac{1.3}{2f}$$ f → supply freq.

Since triggering is controlled only in one half cycle of the supply, this ckt is called half wave RC firing ckt.

By varying R_1 the α can be varied from 0 to 180°

Full wave RC - firing ckt.





Supply to T_1 is given by through uncontrolled rectifier.

Hence both half cycles are +ve half cycles to T_1.

The 'C' starts charging in every half cycle at the beginning.

whenever the V_c reaches $\geq V_g(min)$, T_1 turns-on.

Once T_1 - on, V_c is clamped to zero, till next half cycle.

The 'C' again starts charging from zero.

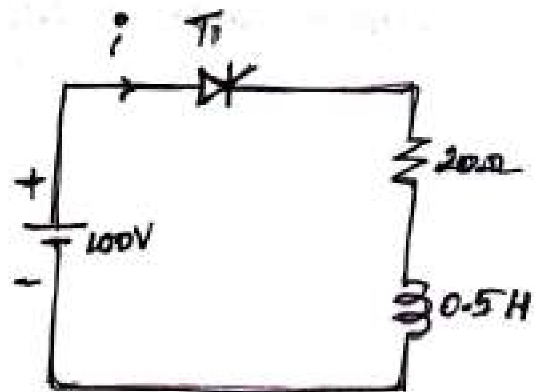
The $\alpha \rightarrow 0$ to $180°$.

triggering controlled in both cycles.

$$RC \geq \frac{0.157}{2\pi f}$$

Max firing angle.

The latching current of a thyristor ckt in fig is 50 mA. The duration of the firing pulse is 50 μs. Will the thyristor get fired?



As the SCR is triggered, the current will rise exponentially in the inductive ckt.

$$\therefore \quad i(t) = \frac{V}{R}\left(1 - e^{-t/\tau}\right)$$

where $\tau = \frac{L}{R}$

Given $L = 0.5\,H$
$R = 20\,\Omega$
$V = 100\,V$
$t = 50\,\mu s$

$$\tau = \frac{0.5}{20} = 0.025 \text{ sec.}$$

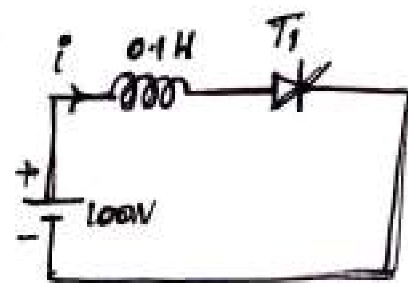
At $t = 50\,\mu s$

$$i(50 \times 10^{-6}) = \frac{100}{20}\left(1 - e^{-\left(\frac{50\times 10^{-6}}{0.025}\right)}\right)$$

$$= 9.99 \text{ mA}$$

Since the calculated circuit current value is less than the given latching c/t value of the SCR, it will not get fired.

If the latching c/t in the ckt shown in fig is 4 mA, obtain the minimum width of the gating pulse required to properly turn-on the SCR.



Given
$L = 0.1\,H$
$V = 100\,V$
$i = 4\,mA$

$i \rightarrow$ latching c/t
$t \rightarrow$ pulse width

The ckt eqn is $\quad V = L\frac{di}{dt}$

$$dt = L\frac{di}{V}$$

Integrating on both sides, $\quad t = \frac{L}{V}i$

$$t_{min} = \frac{0.1}{100}(4 \times 10^{-3})$$

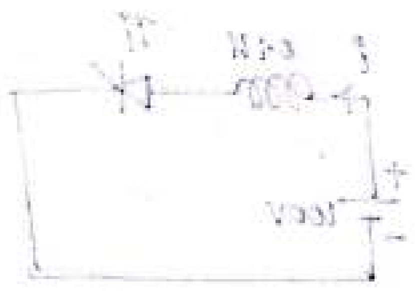
this is the min width of the gating pulse required to turn on SCR $\rightarrow$ $t_{min} = 4\,\mu s$.

3. Compute the peak inverse voltage of thyristor connected in the three phase, 6 pulse bridge ckt having i/p voltage of 415 V. Voltage safety factor is 2.1.

W.K.T $PIV = \sqrt{2}\ V_{in}\ V_f$ $\qquad$ $V_f \rightarrow$ Vol safety factor.

$= \sqrt{2} \times 415 \times 2.1$

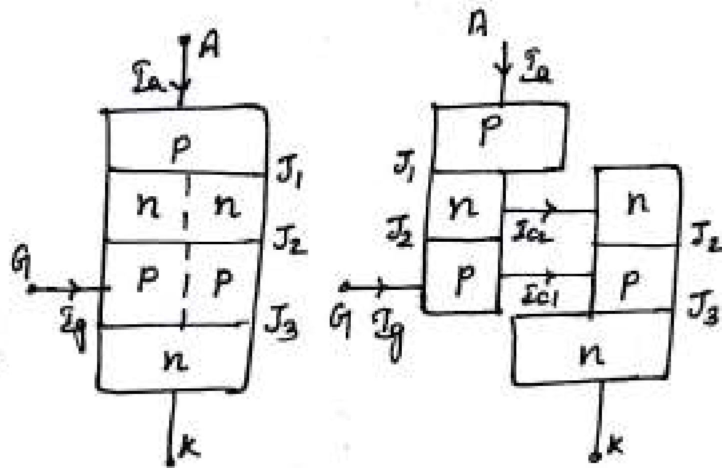
$= 1232.49\ V.$

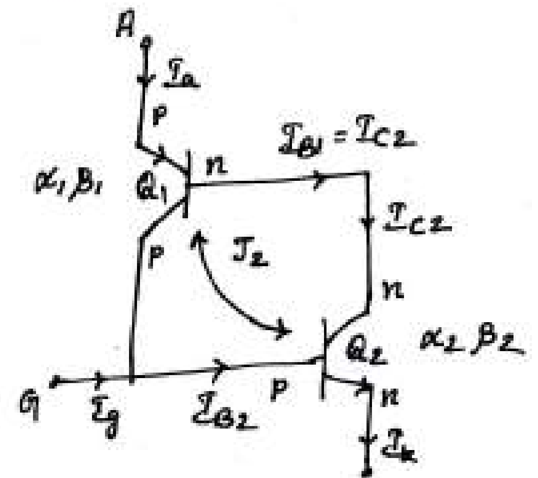


Two transistor model of a thyristor

The regenerative or latching action due to a +ve feedback can be demonstrated by using a two-transistor model of thyristor.

A thyristor can be considered as two complementary transistors, one pnp-transistor Q_1 & other npn-transistor, Q_2.





(a) Thyristor schematic diagram

(b) & (c) Two transistor model of a thyristor.

In off-state, I_C is related to I_E as,

$$I_C = \alpha I_E + I_{CBO}$$

α – Common base current gain.

I_{CBO} – Common base leakage c/.

For Q_1,

$$I_E = I_a \quad \& \quad I_C = I_{C1}$$

$$\therefore \text{For } Q_1, \quad I_{C1} = \alpha_1 I_a + I_{CBO1} \longrightarrow (1)$$

α_1 = Common-base c/ gain of Q_1

I_{CBO1} = Common-base leakage c/ of Q_1

Ilrly for Q_2, $\quad I_{C2} = \alpha_2 I_K + I_{CBO2} \longrightarrow (2)$

α_2 = Common base c/ gain of Q_2

I_{CBO2} = Common base leakage c/ of Q_2

I_K = Emitter c/ of Q_2

① + ② ⇒ $I_a = I_{C1} + I_{C2}$

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 I_k + I_{CBO2} \rightarrow ③$$

When gate sig is applied, then $I_K = I_a + I_g$. → ④

Sub ④ in ③

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 (I_a + I_g) + I_{CBO2}$$

(or) $$I_a = \frac{\alpha_2 I_g + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

For a Si transistor, ch gain α is very low at low emitter ch with an increase in I_E, α builds up rapidly.

With $I_g = 0$ & with thyris FB, $(\alpha_1 + \alpha_2)$ is very low.

Under these condn's, the above eqn shows that fwd leakage ch somewhat more than $(I_{CBO1} + I_{CBO2})$ flow.

If by some means, I_E of both transistors can be led to $\alpha_1 + \alpha_2$ to unity to make the device to turn-on.

Transistor switch:

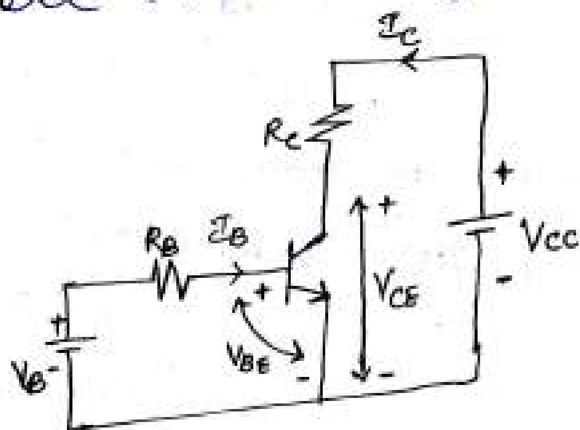
Transistor operates as a switch when it is operated in saturation (or) cut-off region & nowhere else on the load line.

For ideal cases,

transistor operates at point A in sat state as closed switch with $V_{CE} = 0$ & at point B in the cut-off state as an open switch with $I_C = 0$.

In practice, for large I_B, the trans will work in sat region, at pt A with small V_{CES} → on-state vol drop.

When, the base ct is reduced to zero, the device is turned off & it operated in cut off region (operation shift to B')



Applying KVL,

$$V_B - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_B - V_{BE}}{R_B}.$$

Also

$$V_{CC} = V_{CE} + I_C R_C$$

$$V_{CE} = V_{CC} - I_C R_C.$$

But $\beta = \frac{I_C}{I_B}$ $\quad \therefore \quad V_{CE} = V_{CC} - \beta I_B R_C.$

$$= V_{CC} - \beta \left(\frac{V_B - V_{BE}}{R_B} \right) R_C.$$

Also

$$V_{CE} = V_{CB} + V_{BE}$$

$$V_{CB} = V_{CE} - V_{BE}.$$

If V_{CES} is the Collector-Emitter sat vol, then collec ct I_{CS} is given by

$$I_{CS} = \frac{V_{CC} - V_{CES}}{R_C}$$

& the corresponding minimum base current, that produces sat is

$$I_{BS} = \frac{I_{CS}}{\beta}.$$

If $I_B < I_{BS}$, then BJT operates in active region

If $I_B > I_{BS}$, then V_{CES} is almost zero & ∴ $\boxed{I_{CS} = \frac{V_{CC}}{R_C}}$.

This shows that I_C at sat remains substantially const even if I_B is ↑ed.

With $I_B > I_{BS}$, hard drive of transis is obtained. Bcz of this on-state losses will ↑.

Over Drive Factor (ODF)

$$ODF = \frac{I_B}{I_{BS}}$$ (ODF will be as high as 4 or 5).

Forced ct gain $\beta_F = \frac{I_{CS}}{I_B}$ < natural ct gain β

The total power loss in two jns is

$$\boxed{P_T = V_{BE} I_B + V_{CE} I_C}$$

Under sat state, both jn's of Power transis is FB.

Secondary Breakdown (SB) in BJT.

- is a destructive phenomenon, results from the c̄t flow to a small portion of the base, producing localized hotspots.

If the energy in these hot spots is sufficient, the excessive localized heating may damage the transistor.

The 2° breakdown is caused by thermal runaway, resulting from high c̄t concentrations.

The c̄t concentration may be caused by defects in the transistor structure.

The SB occurs at certain combinations of V, I & time.

Bcz the time is involved, the SB is basically an energy dependent phenomenon.

Forward Biased Safe Operating Area (FBSOA)

During ton & on-state condns, the avg jn temp & SB limit the power handling capability of a transistor.

The manufacturers usually provide the FBSOA curves under specified test condns.

FBSOA indicates the $i_c - V_{CE}$ limits of the transistor & for reliable operation of the transistor must not be subjected to greater power dissipation than that shown by FBSOA curve.

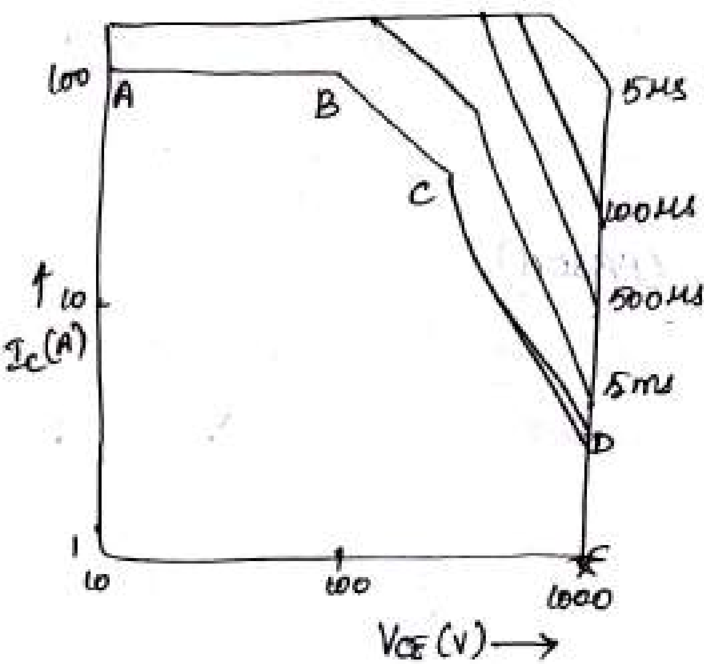
Reverse-biased Safe Operating Area (RBSOA)

During toff, a high cu & high vol must be sustained by the transistor, in most cases with the base to emitter junction reverse biased.

The Collector-Emitter voltage must be held to a safe level at, (or) below, a specified value of collector current.

The manufacturers provide the I_C-V_{CE} limits during reverse-biased turn-off as RBSOA.

FBSOA



RBSOA.