Karpagam College of Engineering, Coimbatore

B.E - EEE

Semester : VI

12E605 - POWER ELECTRONICS

Continuous Internal Assessment - I

Answer key.

Part - A

A1. Define Latching current & Holding current of SCR.

Latching current (I_L)

The latching current is the minimum forward current that flows through the SCR to keep it in forward conduction mode at the time of triggering. Removal of gate current doesnot affect the conduction of anode current. (1)

Holding current (I_h)

✓ This is associated with turn-off process.

✓ The SCR will return to its original forward blocking state if the anode current falls below a low-level, called the holding current. (1)

A2. Based on the controllability, the power semiconductor devices are classified into

✓ Uncontrollable devices - Eg : diode

✓ Partially controllable devices - Eg : SCR

✓ Fully controllable devices - Eg : BJTs, MOSFETs, GTOs, IGBTs, SITs etc., (2)

A3. Advantages of IGBT over MOSFET

✓ IGBTs have low on-state losses compared to MOSFETs.

✓ IGBTs have flat temperature co-efficient.

✓ IGBTs are available with high power ratings compared to MOSFETs.

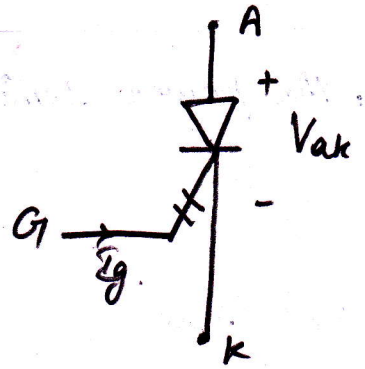
✓ Current sharing in multiple paralleled IGBTs is far better than power MOSFETs. (2)

A4

✓ Conduction losses are the losses that occur when the device is in full conduction. These losses are in direct relationship with duty cycle. (1)

✓ Switching losses are the losses the occur when the device is transitioning from the blocking state to the conducting state & vice versa. (1)

A5. Symbol of IGCT



(1)

Applications of Igct.

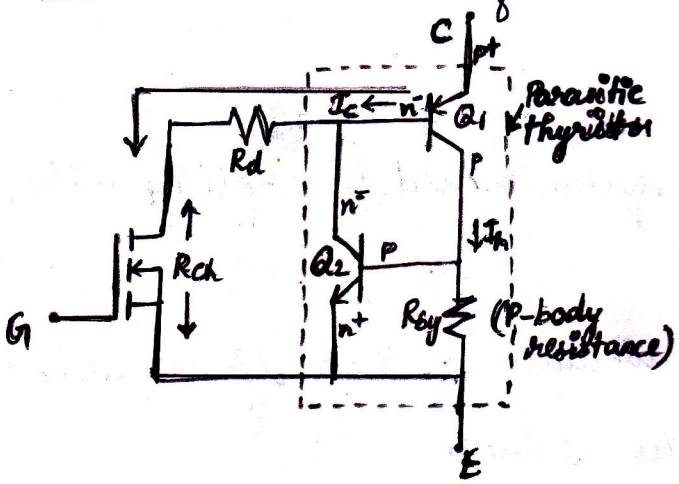
Used in areas such as medium voltage drive and transmission & distribution. (1)

SOA of BJT & its significance.

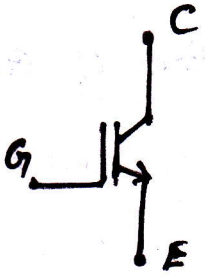
✓ The safe operating area (SOA) of the BJT is the area on the $i_c - V_{CE}$ plane where BJT should be operated.

✓ It gives the combinations of current and voltage where the device functions safely without any damage. (2)

A7. Two transistor model of IGBT



Circuit Symbol.



(2)

A8. Advantages and disadvantages of TRIAC

✓ Triacs can be triggered with positive or negative polarity voltages.

✓ A triac needs a single heat sink of slightly larger size, whereas anti-parallel thyristor needs two heat sinks of slightly smaller size.

✓ A Triac needs a single fuse for protection, which simplifies construction. (1)

any (2)

✓ Triacs have low dv/dt rating compared to SCRs

✓ Reliability of Triacs is less than that of SCRs.

✓ SCRs are available in larger rating compared to TRIACs. (1)

✓ A trigger circuit with Triac needs careful consideration.

any (2)

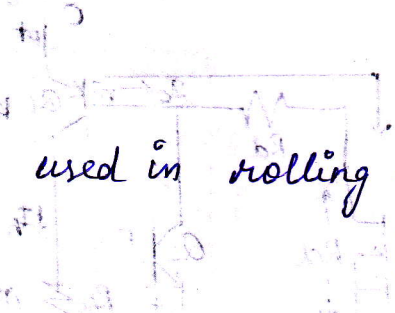
A9. **Commutation**

It is defined as the process of turning-off a thyristor.

Types - Natural Commutation

Forced Commutation. (2)

A10. Four applications of GTO.



✓ In high performance drive systems used in rolling mills, robotics, machine tools etc.,

✓ used for traction purpose because of their lighter weight

✓ Adjustable-frequency inverter drives

✓ Used in low power applications.

✓ Induction heating etc.,

(2)

any (4)

Part - B.

B1.

(a) i) Given:

Latching current $I_L = 50\,mA$.

$L = 0.5\,H$

$R = 20\,\Omega$

$t = 50\,\mu s$. $\quad V = 100\,V$.

$$i(t) = \frac{V}{R}\cdot(1 - e^{-t/\tau})$$

where $\tau = \frac{L}{R} = \frac{0.5}{20} = 0.025$ sec.

$$i(50\times10^{-6}) = \frac{100}{20}\left[1 - e^{\left(\frac{-50\times10^{-6}}{0.025}\right)}\right]$$

$5(1-e^{-\frac{25\times10^{-3}}{0.025}})$

$5(1-e^{-0.1})$

$= 9.99\,mA.$ (4)

Since, the calculated circuit current value is less than the given latching current of SCR, the device will not get fired.

$$V = Ri + L\frac{di}{dt} \Rightarrow i = \frac{V}{R}(1 - e^{-t/\tau})$$

$$50\times10^{-3} = \frac{100}{20}(1 - e^{-t/0.025})$$

$$\frac{50\times10^{-3}}{5} = (1 - e^{-40t})$$

$$0.01 = 1 - e^{-40t}$$

$$0.99 = e^{-40t}$$

$$\ln(0.99) = -40t$$

$$-0.01 = -40t$$

$$t = 0.00025\,sec$$

$$t = 0.25\,ms$$ (4)

B1.
a) ii) Comparison of GTO with SCR

GTO has the following advantages & disadvantages with SCR.

(i) Magnitude of latching & holding current is more in GTO.

(ii) On-state voltage drop and the associated loss is more in GTO.

iii) Triggering gate current is higher than that required for conventional thyristor.

iv) Gate drive circuit losses are more in GTO.

v) GTO has faster switching speed.

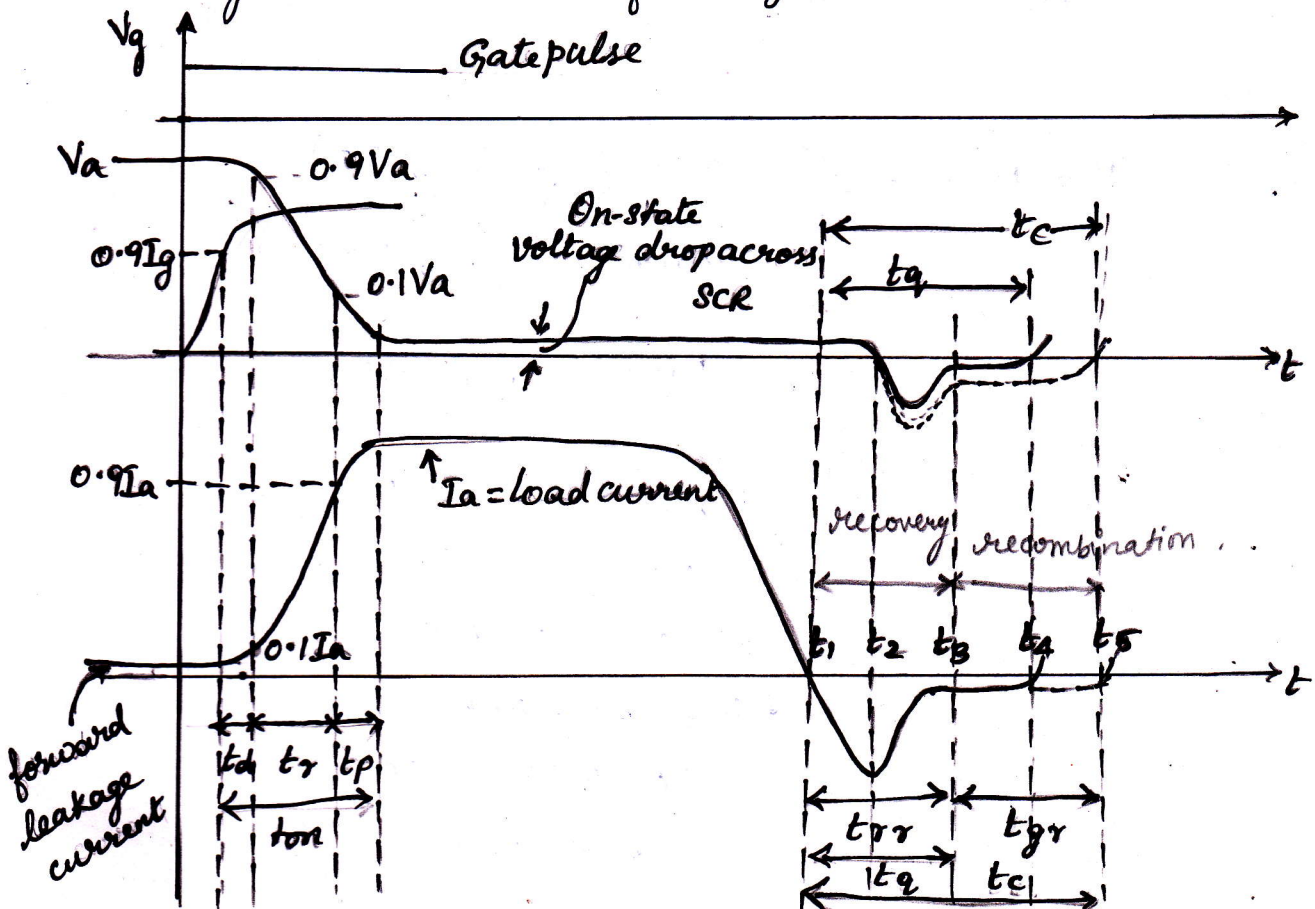
vi) GTO has more di/dt rating at turn-on.

vii) GTO unit has higher efficiency

viii) GTO has reduced acoustical and electromagnetic noise due to elimination of commutation chokes.

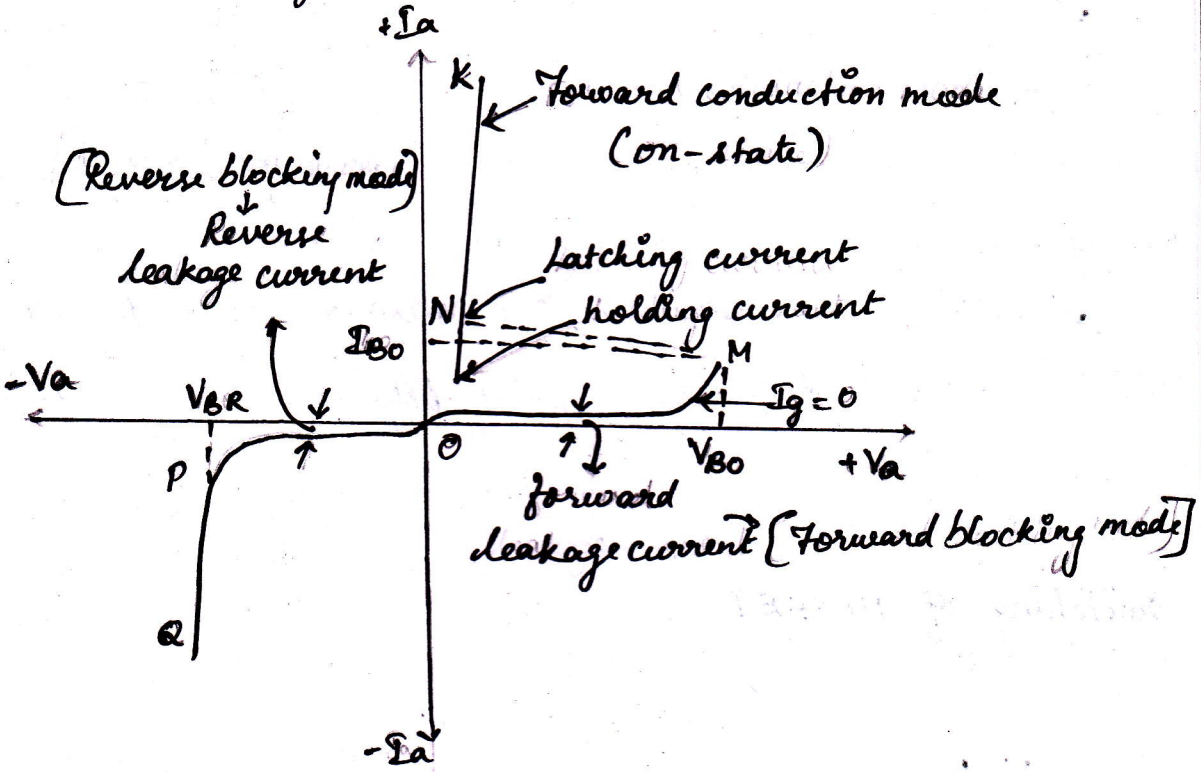
(4)

B1.
a) iii) Switching Characteristics of a thyristor.



(3)

i) VI Characteristics of a Thyristor



(2)

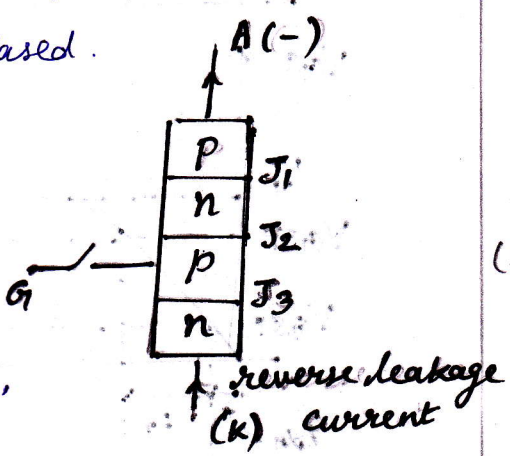
The thyristor has 3 basic modes of operation.

1. Reverse blocking mode

✓ When Cathode is made +ve with respect to anode with switch S open, the thyristor is reverse biased.

Junctions J1, J3 – Reverse biased

J2 – Forward biased.

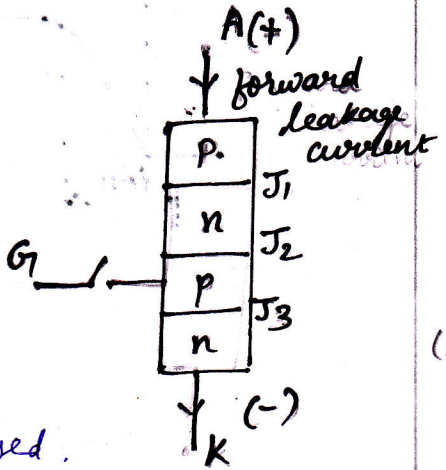


(1)

✓ A small leakage current of a few mA flows. If the reverse voltage is increased, then at a critical breakdown called reverse breakdown voltage V_{BR}, an avalanche occurs at J1 & J3 & the reverse current increases rapidly.

2. Forward blocking mode.

✓ When anode is made +ve with respect to cathode, with gate open, thyristor is said to be forward biased.



(1)

✓ J1, J3 – Forward biased J2 – Reverse biased.

In this mode, a small current, called forward leakage current flows.

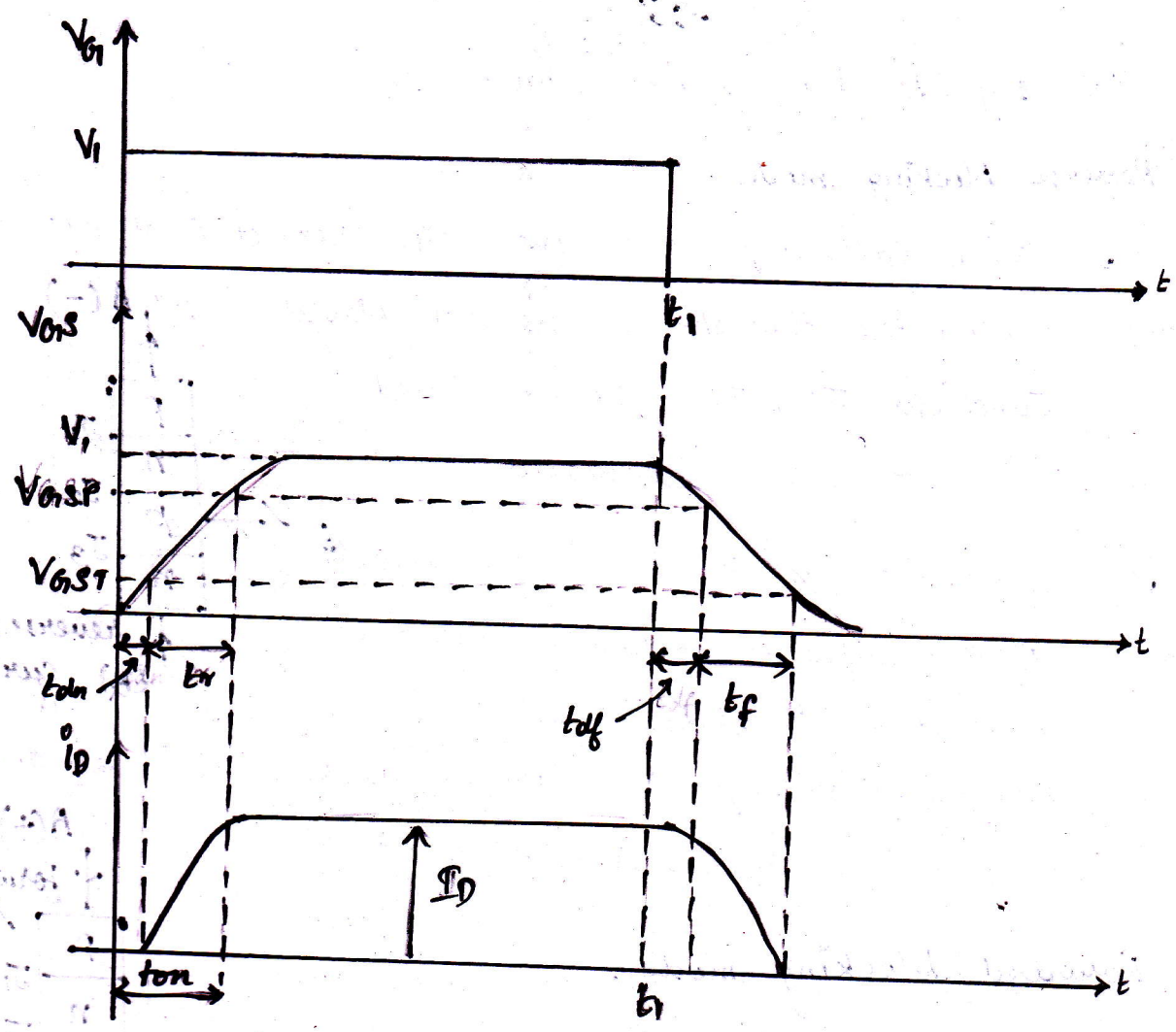
(4)

3. Foward Conduction mode

✓ When anode to cathode foward voltage is increased with gate circuit open, reverse biased junction J_2 will have an avalanche breakdown at a voltage called forward breakover voltage V_{BO}.

✓ After this breakdown, SCR turned on with point H at once shifting to N & then to a point anywhere between N & K. (1)

B1.
b) ii) Switching of MOSFET



(2)

✓ The switching characteristics of a power MOSFET are influenced to a large extent by the internal capacitance of the device & the internal impedance of the gate drive circuit.

✓ At turn-on, there is an initial delay t_{dn} during which i/p capacitance charges to gate threshold voltage V_{GST}.

✓ t_{dn} → turn-on delay time.

✓ There is further delay t_r, called rise time, during which gate voltage rises to V_{GSP}, a voltage sufficient to drive the MOSFET into on state.

✓ During t_r, drain current rises from zero to full-on current I_D.

Thus, the total turn-on time is (2)

$$t_{on} = t_{dn} + t_r.$$

✓ As MOSFET is a majority carrier device, turn-off process is initiated soon after removal of gate voltage at time t_1.

✓ The turn-off delay time, t_{df} is the time during which i/p capacitance discharges from over-drive gate voltage V_1 to V_{GSP}.

✓ The fall time, t_f is the time during which i/p capacitance discharges from ~~over drive~~ ~~gate voltage~~ ~~V_1~~ ~~to~~ V_{GSP} to threshold voltage.

✓ During t_f, drain current falls from I_D to zero.

∴ So when $V_{GS} \leq V_{GST}$, PMOSFET turn-off is complete (2)

B1.

b) iii) Comparison of PMOSFET with BJT

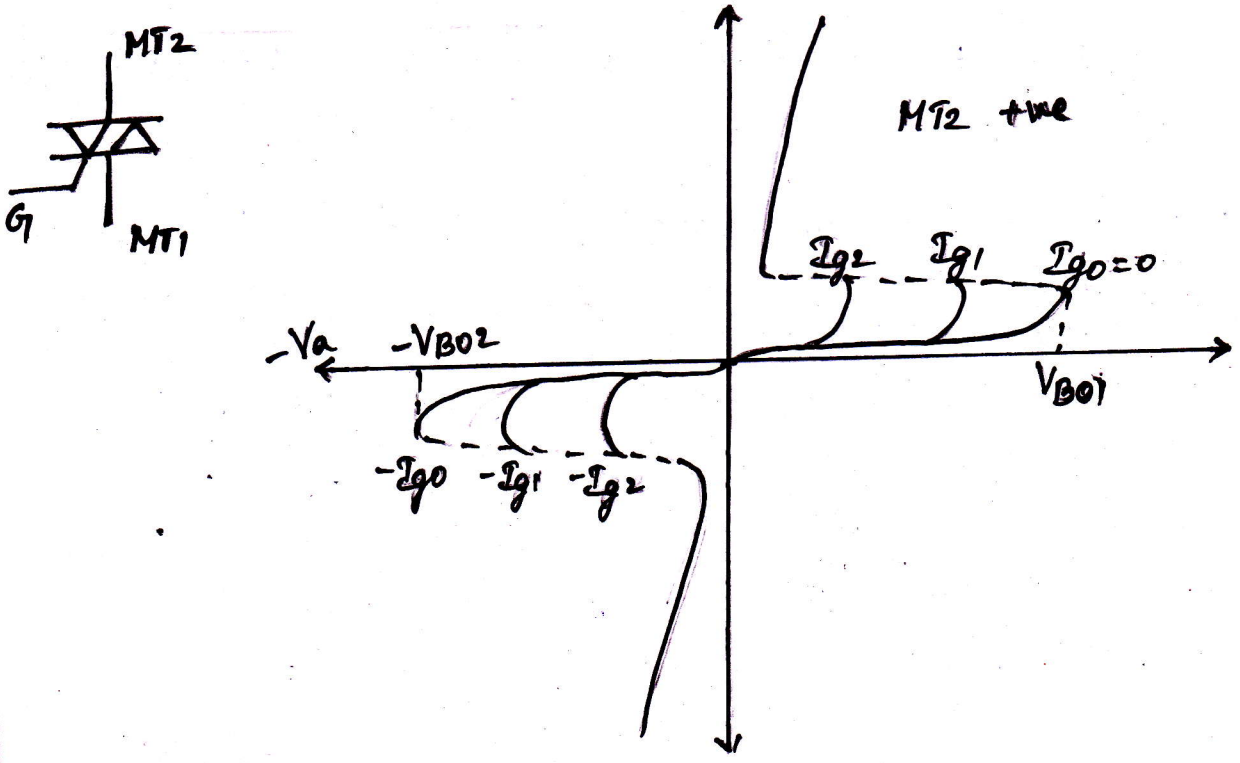
BJT	PMOSFET
1) Bipolar device	1) Unipolar device.
2) Low i/p impedance	2) High i/p impedance.
3) Higher switching losses	3) Has lower switching losses but its on-resistance & Conduction losses are more.
4) Current controlled device	4) Voltage controlled device.
5) has negative temperature co-efficient for resistance	5) has positive temperature co-efficient for resistance.
6) has secondary breakdown problem.	6) no secondary breakdown problem.
7) Available with ratings upto 1200V, 800A	7) Available with ratings upto 500V, 140A.

(4)

B2)

a) i) Different modes of Operation & VI characteristics of TRIAC.

TRIAC is a bidirectional device with 3 terminals. It can conduct in both the directions.

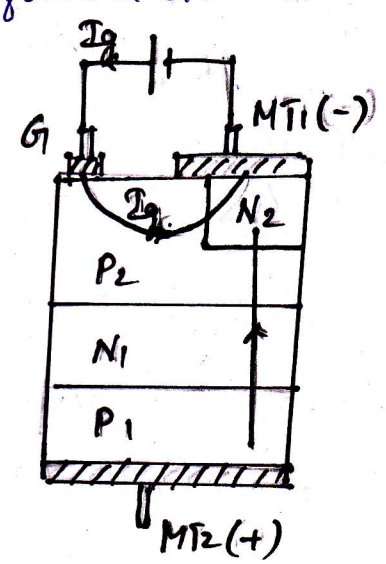


(2)

The turn-on process of a triac can be explained as under:

(i) MT2 - (+)ve MT1 - (-)ve Gate - (+)ve

✓ The junctions P_1N_1, P_2N_2 are forward biased but junction N_1P_2 is reverse biased.



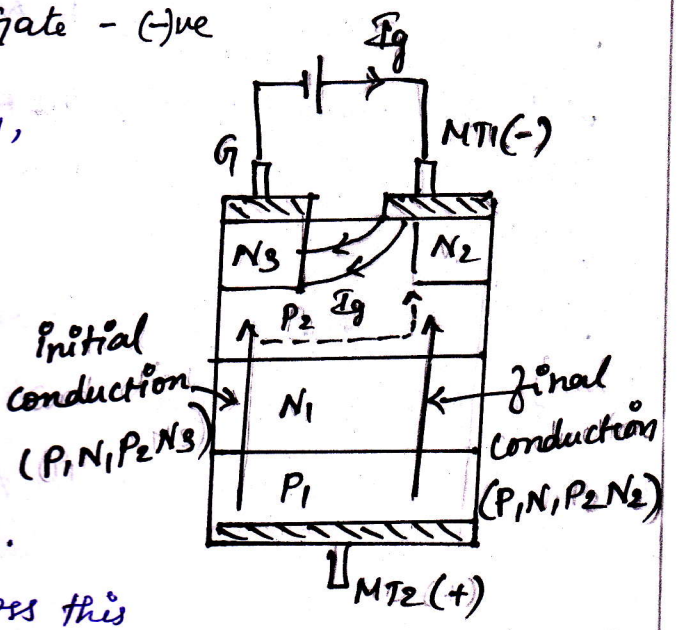
✓ When Gate is +ve w.r.to MT1, gate current flows mainly through P_2N_2.

✓ When sufficient charge is injected in P_2 layer, reversed biased junction N_1P_2 breaks.

✓ Triac starts conducting through $P_1N_1P_2N_2$ layers.

∴ The device is more sensitive in this mode.

(ii) MT2 - (+)ve MT1 - (-)ve Gate - (-)ve



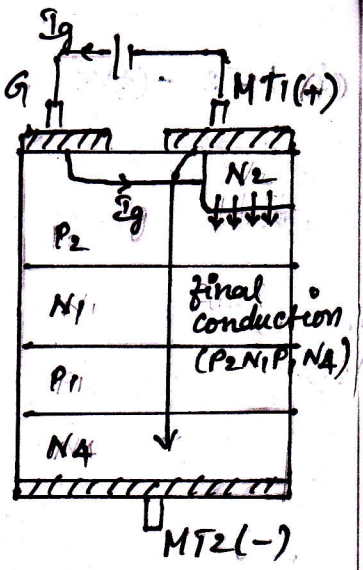
✓ When gate is -ve w.r.to MT1, the Ig flows through P_2N_3 jn & reversed biased junction N_1P_2 is forward biased.

✓ So, triac starts conducting through $P_1N_1P_2N_3$ layers initially.

✓ As so, the voltage drop across this path falls by potential blw P_2N_3 rises towards MT2.

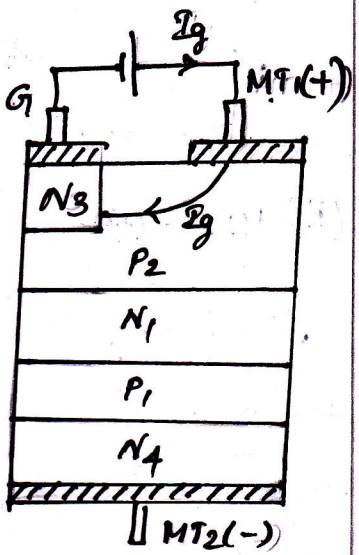
✓ As a consequence, right hand part of triac consisting of main structure $P_1N_1P_2N_2$ begins to conduct.

(iii) MT_2 - (-)ve MT_1 - (-)ve Gate - (+)ve



- ✓ The I_g foward biases $P_2 N_2$ junction
- ✓ N_2 Layer injects e's into P_2 layer.
- ✓ So that, junction $N_1 P_1$ breaks.
- ✓ Eventually the structure $P_2 N_1 P_1 N_4$ is completely turned on.
- ✓ As the triac is turned on by remote gate N_2, the device is less sensitive in 3rd quadrant with gate -ve.

(iv) MT_2 - (-)ve MT_1 - (+)ve Gate - (-)ve

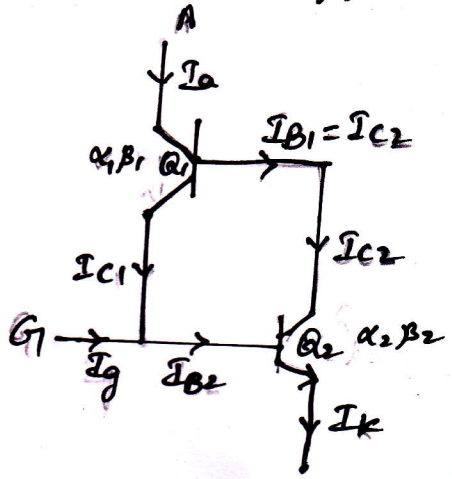


- ✓ In this mode, N_3 acts as a remote gate.
- ✓ The I_g flows from P_2 to N_3.
- ✓ Reverse biased junction $N_1 P_1$ is broken & finally the structure $P_2 N_1 P_1 N_4$ is turn on completely.
- ✓ Though the triac is turned on by remote gate N_3 in third quadrant, yet the device is more sensitive under this condition.

(5)

B2.

a) ii) Condition for the occurrance of latch up in SCR using two transistor analogy.



I_k - emitter current of Q_2

I_c - Collector current

α - Common-base current gain

I_{CBO} - Common-base leakage current.

I_a - anode current

I_c - Collector current

(12)

In the off-state of a transistor, I_C is related to I_E as

$$I_C = \alpha I_E + I_{CBO} \longrightarrow (1)$$

For transistor Q_1, $I_E = I_a$ & $I_C = I_{C1}$

$\therefore$ For Q_1, $I_{C1} = \alpha_1 I_a + I_{CBO1} \longrightarrow (2)$

Similarly for Q_2, I_{C2} is given by

$$I_{C2} = \alpha_2 I_k + I_{CBO2} \longrightarrow (3)$$

$$I_{C1} + I_{C2} = I_a$$

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 I_k + I_{CBO2} \longrightarrow (4)$$

When gate current is applied, then $I_k = I_a + I_g \longrightarrow (5)$

Sub (5) in (4)

$$\therefore I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 (I_a + I_g) + I_{CBO2}$$

$$\boxed{I_a = \frac{\alpha_2 I_g + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}} \Rightarrow \boxed{I_a = \frac{\alpha_2 I_g}{1 - (\alpha_1 + \alpha_2)}}$$

(4)

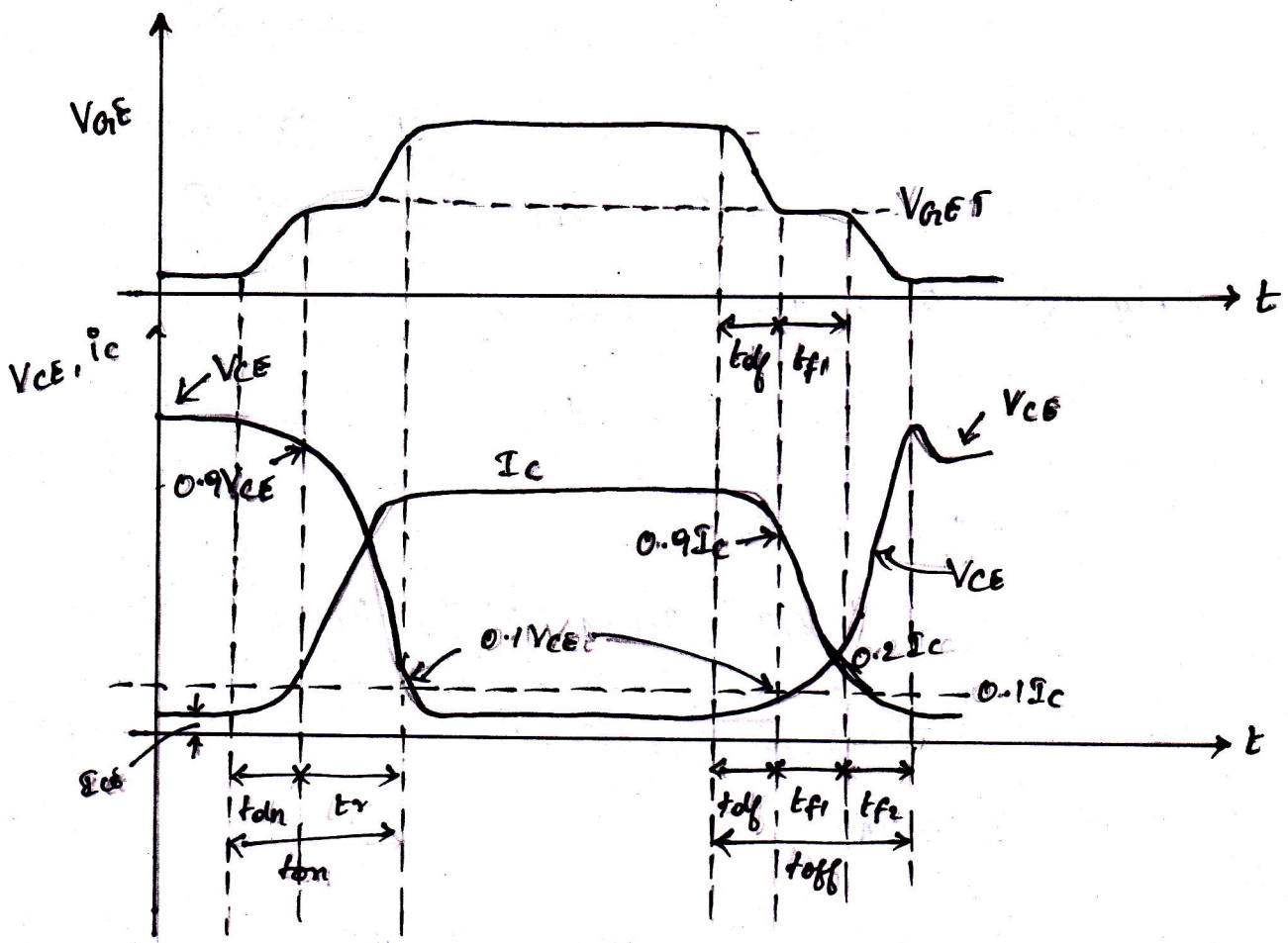
B2.
a) iii) Difference between TRIAC and SCR

SCR	TRIAC.
Can be triggered only with positive voltage	Can be triggered with +ve or -ve polarity voltages.
Needs heat sinks of smaller size.	requires single heat sink of slightly larger size.
possesses high $\frac{dv}{dt}$ rating	low dv/dt rating.
high reliability	not reliable.
operates in only one direction	operates in both directions.

(4)

B2.

b) i) Switching performance of IGBT.



(2)

Turn-on time

It is the time between the instants of forward blocking to forward on-state.

Ton time is composed of delay time tdn & rise time tr.

$$t_{on} = t_{dn} + t_r$$

Delay time (t_{dn})

defined as the time for collector emitter voltage to fall from V_{CE} to $0.9V_{CE}$. Also defined as collector current to rise from I_{CE} to $0.1I_C$.

Rise time (t_r)

time during V_{CE} falls from $0.9V_{CE}$ to $0.1V_{CE}$.

also can be defined as the time for I_C to rise from $0.1I_C$ to final value I_C.

Turn-off time

It consists of 3 intervals delay time (t_{df}), initial fall time (t_{f1}) and final fall time (t_{f2})

ie, $\Rightarrow$ $\boxed{t_{off} = t_{df} + t_{f1} + t_{f2}}$

Delay time (t_{df})

It is the time during which gate voltage falls from V_{GG} to threshold voltage V_{GGT} also collector current falls from I_C to $0.9 I_C$.

At the end of t_{df}, V_{CE} begins to rise.

First fall time (t_{f1})

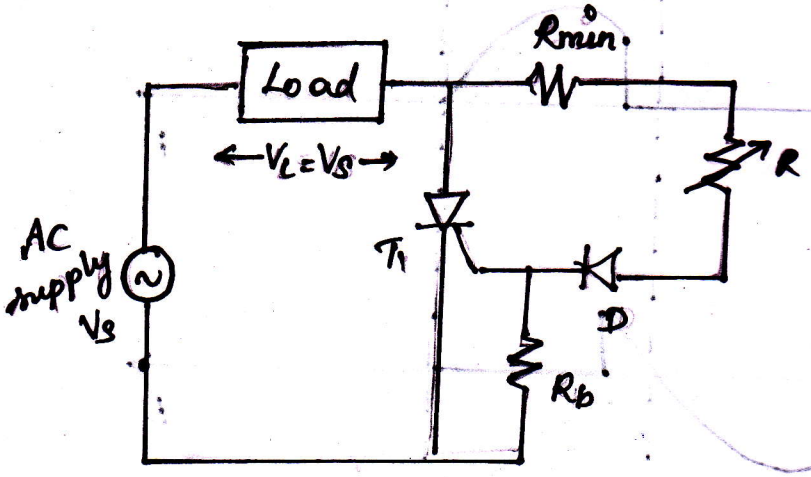
defined as the time during which I_C falls from 90% of its value to 20% also V_{CE} rises from its initial value to $0.1 V_{CE}$.

Final fall time (t_{f2})

defined as the time during which I_C falls from 20 to 10%. Also V_{CE} rises from $0.1 V_{CE}$ to final value of V_{CE}

(3)

B2. b) ii) Resistance firing circuit for triggering SCR's.



(1)

(15)

The circuit operation as follows.

i) As V_s goes positive, SCR is forward biased, however it will not conduct ($V_L = 0$) until its gate current exceeds $I_{g(min)}$

ii) The +ve V_s also forward biases the diode and the SCR's gate-cathode junction; this causes flow of i_g.

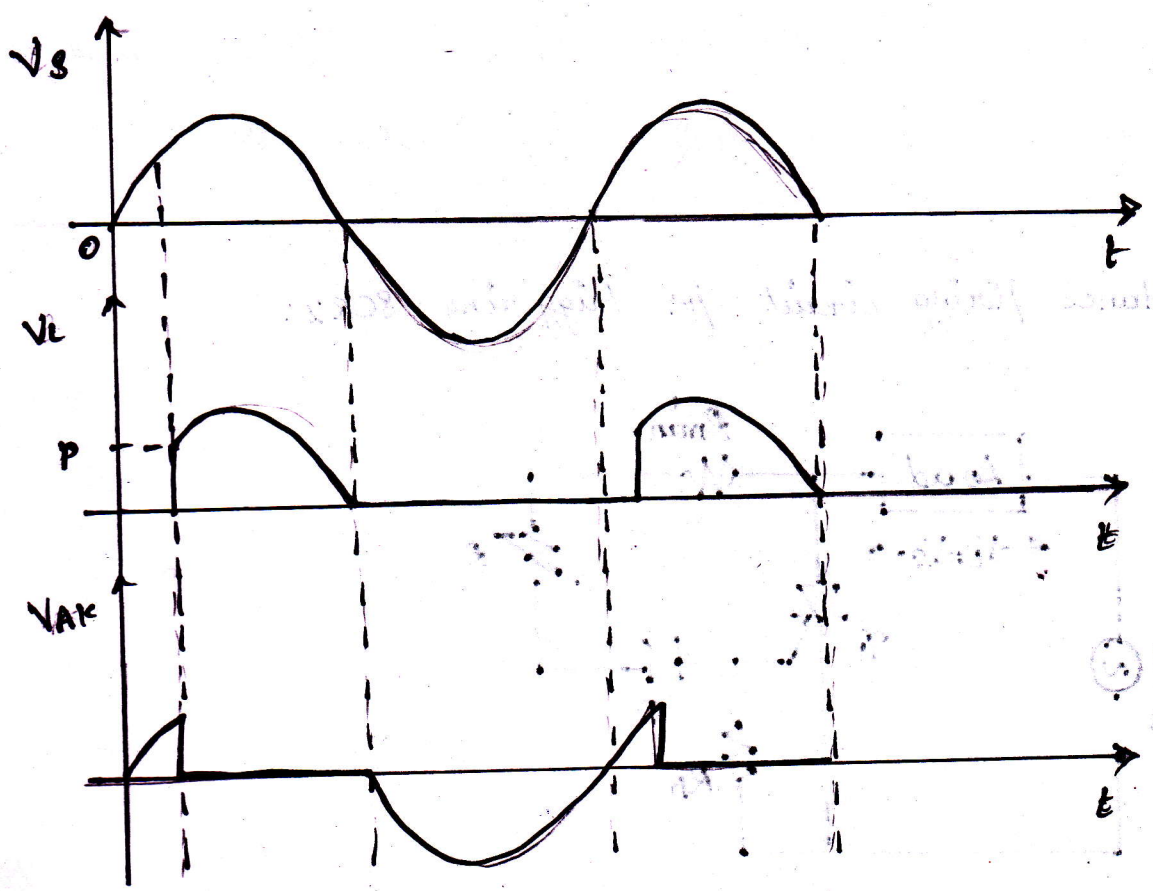
iii) When i_g reaches $I_{g(min)}$, the SCR turns "on" & $V_L \approx V_s$.

iv) The SCR remains on & $V_L \approx V_s$ until V_s decreases to the point where the load current is below the SCR holding current.

v) The SCR now turns "off" & remains "off" while V_s goes negative since its anode-cathode is reverse biased. & so $V_L = 0$

vi) The diode in the ckt is to prevent the gate-cathode reverse bias from exceeding peak reverse gate vol during -ve half cycle. (Diode Peak rev vol rating > i/p vol V_{max}) (1)

vii) The cycle repeats.



(2)

✓ The load voltage wave can be controlled by varying Resistance R.

✓ If R is increased, the gate current will reach its trigger value $I_{g(min)}$ at a greater value of V_s.

✓ Thus, the triggering angle α will increase & if R is decreased α will decrease.

✓ R_{min}, Limiting resistor is placed between anode & gate so that the peak gate current of thyristor (I_{gm}) is not exceeded.

$$R_{min} \geq \frac{V_{max}}{I_{gm}}$$

✓ Stabilising resistor R_b should have such a value that the max vol drop across it does not exceed max gate voltage $V_{g(max)}$.

$$R_b \leq \frac{(R + R_{min})\, V_{g(max)}}{(V_{max} - V_{g(max)})} \longrightarrow (1)$$

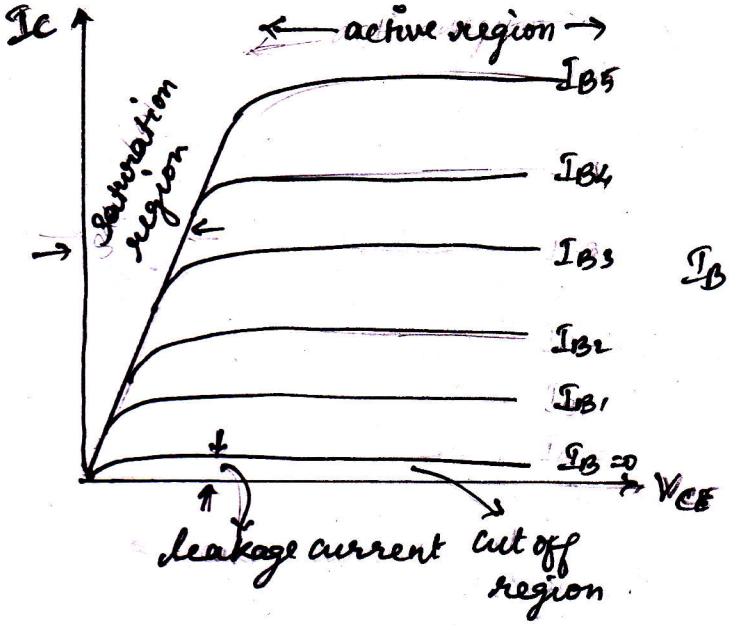
✓ The trigger angle α is greatly dependent on SCR's $I_{g(min)}$, & is also highly temperature dependent.

✓ The value of α can be varied only upto an approximate value of 90° with this circuit.

✓ This is because V_s is maximum at its 90° & I_g has to reach $I_{g(min)}$ somewhere between (0-90°). (1)

(17)

B2. b)
iii) Output Characteristics of BJT.



$I_{BN} > I_{B4} > I_{B3} > I_{B2} > I_{B1}$

(1)

There are 3 operating regions of a transistor.

Cut-off region

✓ In this region, the transistor is off or the base current is enough to turn it on & both junctions are reverse biased.

✓ For zero base current, ie, $I_B = 0$, as V_{CE} is increased, a small leakage current exists.

Active region

✓ In this region, the transistor acts as an amplifier, where the base current is amplified by a gain & V_{CE} decreases with I_b.

✓ The collector base junction is Reversebiased & base-emitter junction is forward biased

Saturation region

✓ Both junctions collector-base & Base-emitter are forward biased.

✓ The base current is sufficiently high so that the collector voltage is low & the transistor acts as a switch.

(3)

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \quad ; \quad I_B = \frac{V_B - V_{BE}}{R_B}.$$

M.K
Staff Incharge 28/12/15

V. Chandrasekar 29/12/15
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