Protection & Cooling of Power switching devices

Introduction.

All power devices have limited operating capabilities.

Reliable & satisfactory use of devices depends on ensuring that the circuit conditions imposed on them are always within their capabilities.

To achieve this, device has to be surrounded by components chosen to protect it against the extreme condns, enabling an economic & easily obtainable device to be used.

If a device experiences over-vol, overload, high ckt or voltage transients, high device temp or other abnormal operating condns, the device may be degraded in performance or destroyed permanently.

The device should be protected against abnormal condns for satisfactory & reliable operation so that it faithfully adheres to the specified characteristics of the manufacturer.

To operate the device within its upper temperature limit, the heat produced by losses in a device must be dissipated sufficiently & effectively.

Therefore, heat sink & cooling arrangement for devices are employed.

Overvoltage conditions.

Devices can be damaged by excessive vol applied even for very short periods of time.

There are many such transient condns in all power electronic ckts & it is necessary to understand them to ensure satisfactory protection.

The conditions most important to power-electronic ckts are:

(i) Lightning surges (ii) Transformer switching

(iii) Thyristor turn-off (iv) Load switching, etc.,

Lightning Surges.

Lightning strikes on overhead power-lines can be passed through the supply n/w & appear on all power-electronic ckts which are directly connected to the n/w.

They are usually attenuated by supply system transformers & lightning arrestors but can still be many times the normal vol level lasting for periods up to tens of μsec.

Fortunately, their magnitude tends to reduce as the time of the transient ↑s.

In some applications, the o/p connections from the thyristor ckt may be exposed to lightning.

eg: dc transmission & traction, & o/p vol suppression ckts will then be needed.

Transformer switching

It is a regular & significant source of transient overvoltages, particularly when a thyristor equipment is supplied by its own transformer.

Transients will occur on the secondary windings when its 1° ckt is opened or closed.

These occur even when the equipment & transformer are unloaded due to the magnetizing condn's within the transformer.

When the supply is closed on to the transformer, the inrush magnetizing ckt causes vol of upto twice the normal to occur transiently.

Capacitive coupling b/w the 1° & 2° can temporarily boost the 2° voltage if the transformer has a large step-down ratio. Refer fig a to c.

Power device turn-off

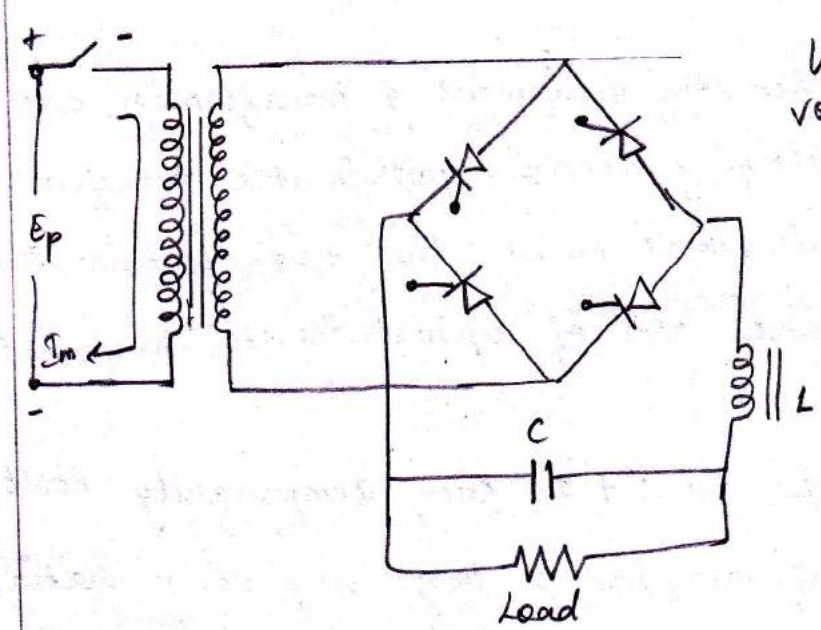
When any device turn-off at a relatively high rate of change of ckt, a reverse ckt will flow to sweep away the stored charge.

Once this has been achieved the ckt quickly reduces to zero, inducing high voltages in the ckt inductances.

These vol can be extremely high if no protection is included to limit them; they appear as reverse voltage across the device which are turning off, & they are reflected onto other devices in the ckt in both polarities.

The stored charge & hence, the level of reverse charge re... C_j varies b/w thyristors & due to temperature, such max values shave to be used in assessing protection requirements.

Voltage transient due to interruption of transformer magnetizing current



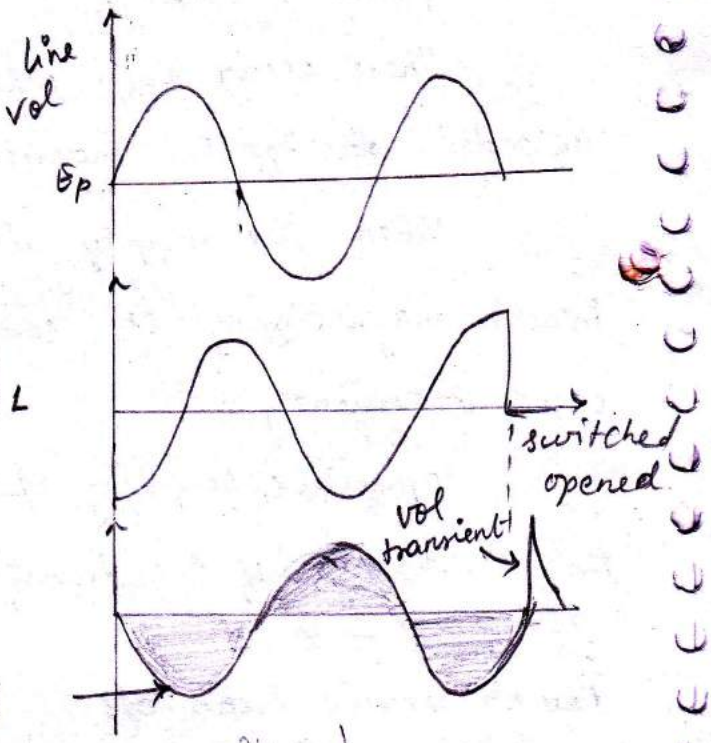
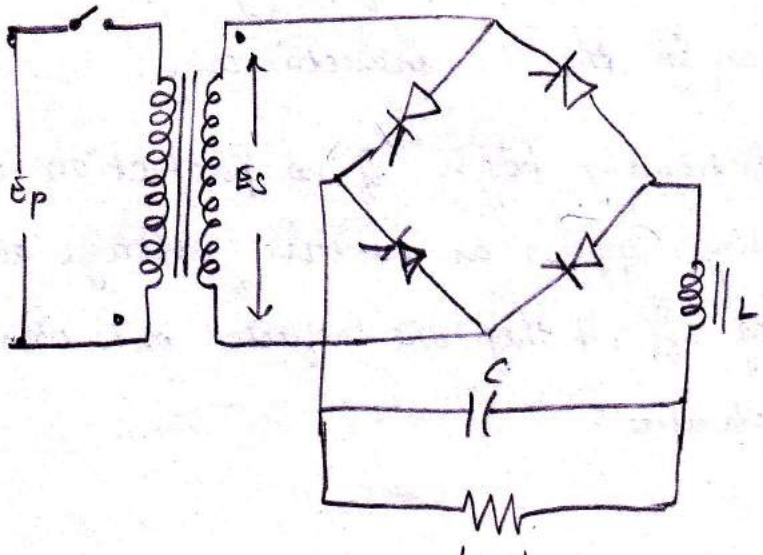


fig (a)

Voltage transient due to energizing transformer primary



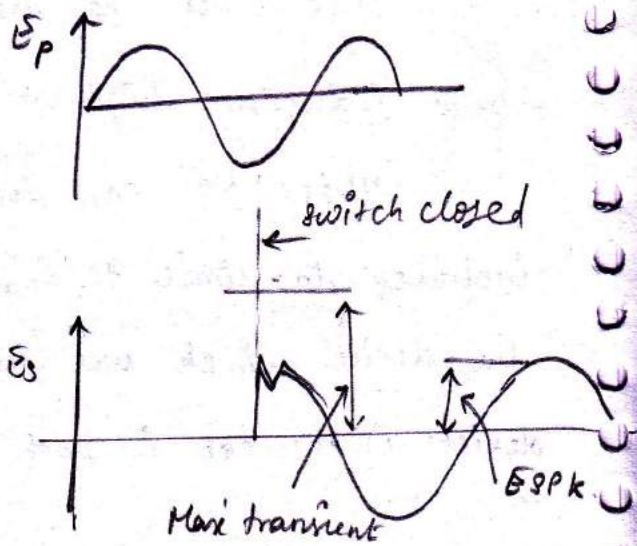
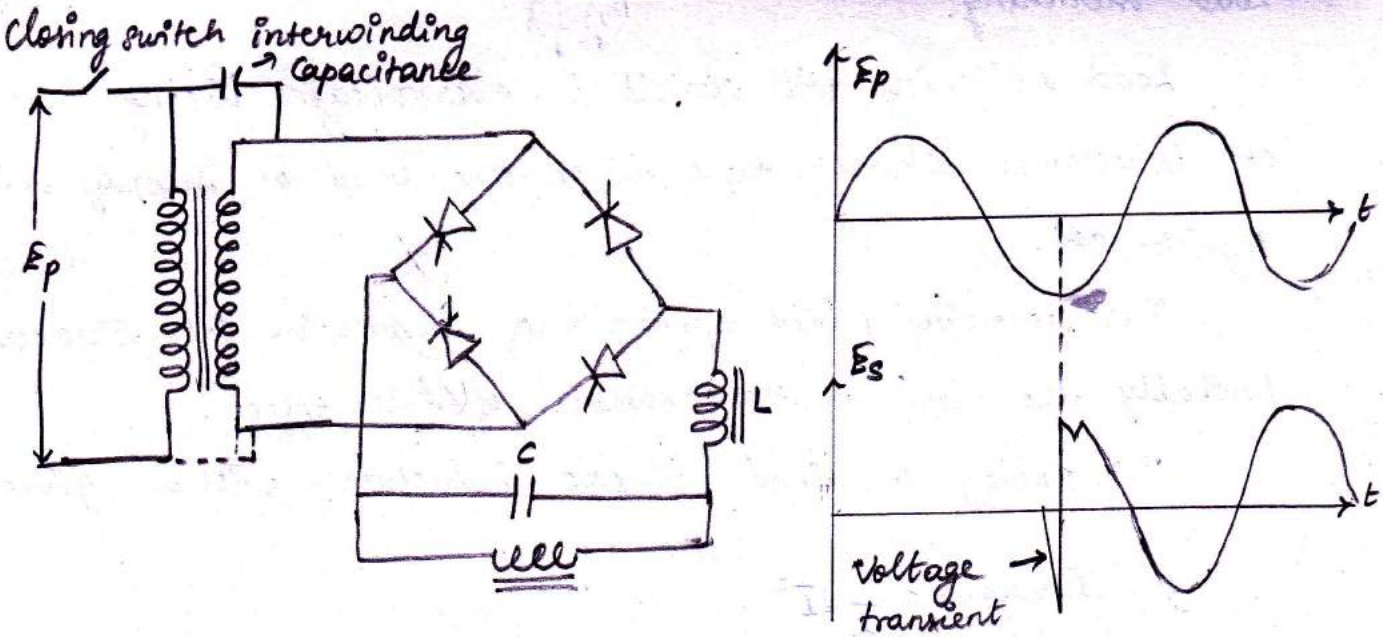
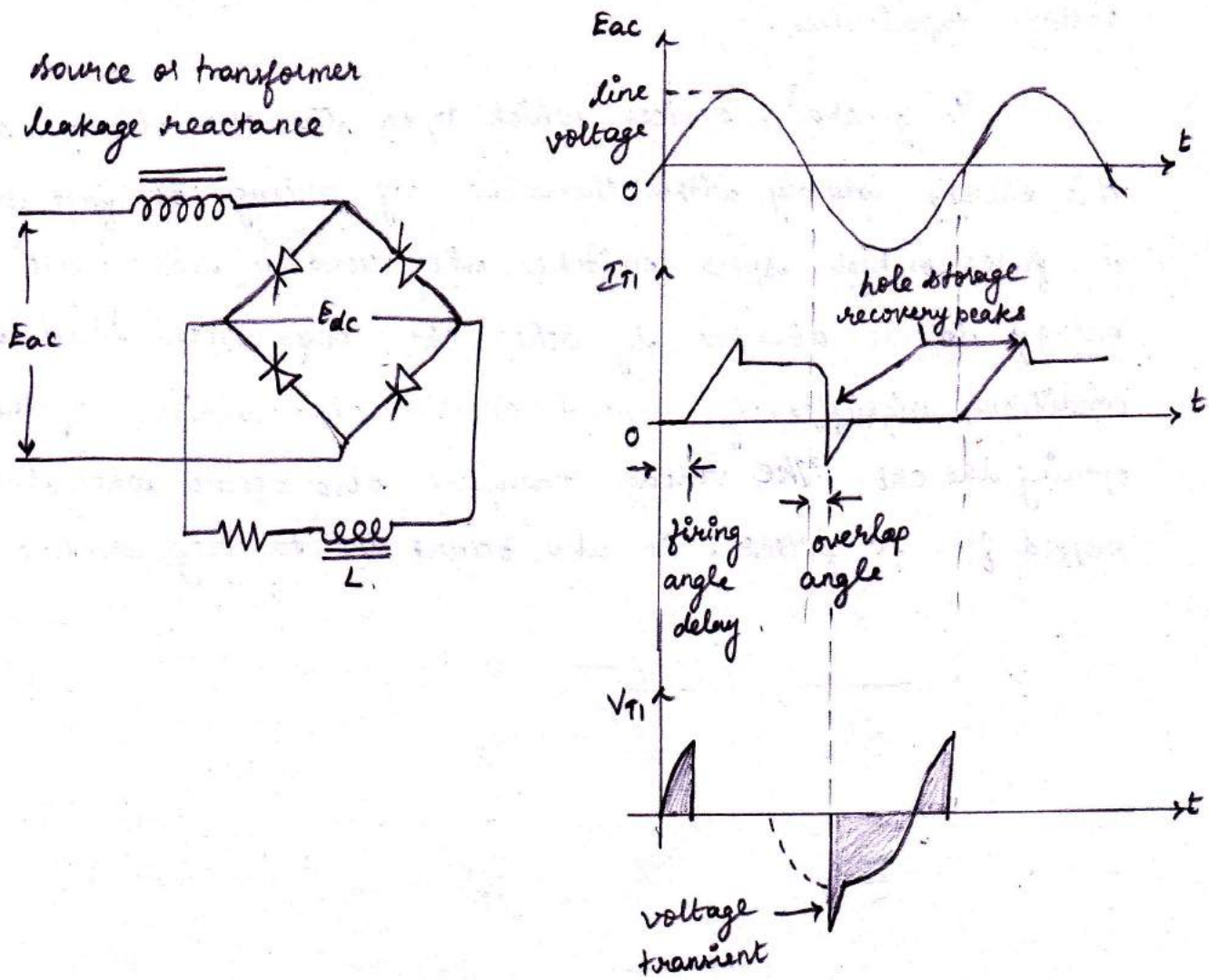


fig (b)



Voltage transient due to energizing step-down transformers fig (c)



fig(d) Transients due to reverse recovery of SCRs.

Load switching.

Load switching will result in overvoltages being induced in ckt inductances whether these be on the load or supply side of the thyristor ckt.

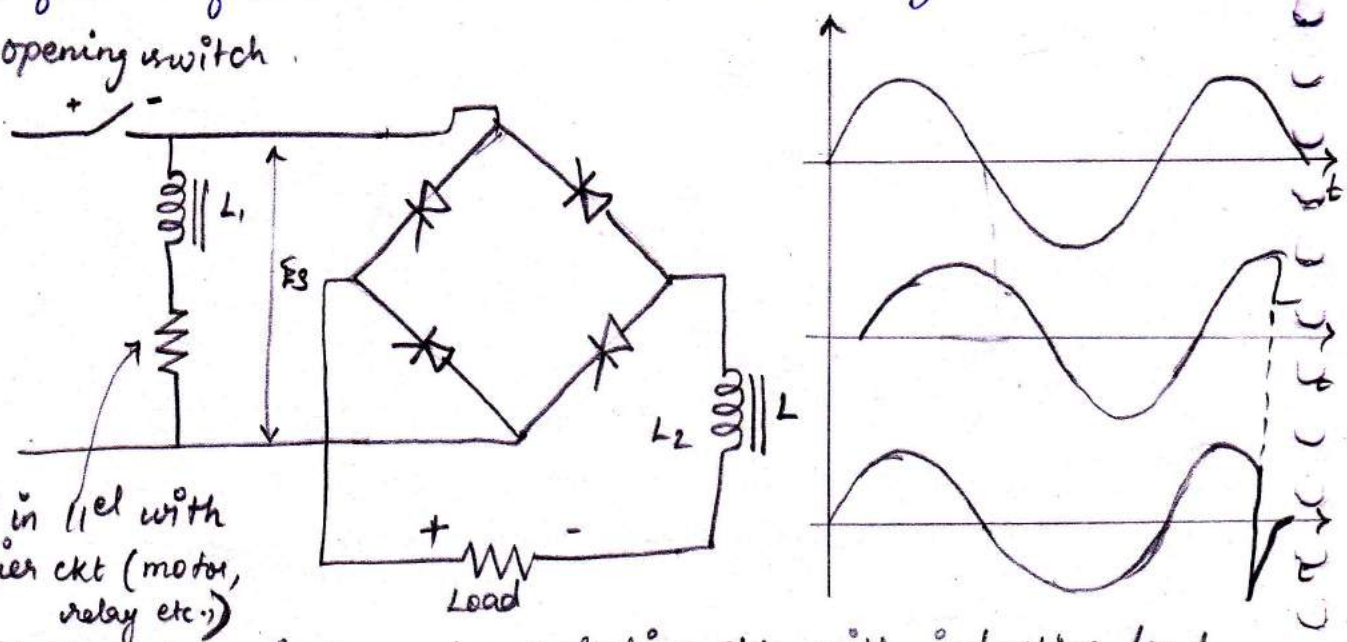
Fuse blowing & the operation of protective ckt breakers are probably the most severe examples of this effect.

The energy contained in ckt inductances will be given by

$$\text{Energy} = \frac{1}{2} LI^2.$$

where I is the ckt flowing & this will need to be dissipated in the protective components used, without exceeding the device voltage capabilities.

In general, devices which open the ckt slowly, dissipate this energy slowly within themselves by arcing or fast switches, ie, fuses or high speed switches, will usually leave most of the energy to be absorbed by other ckt components. Load switching conditions significantly depend on the characteristics of the switch opening the ckt. The voltage transient also occurs when the load dropped from LC filter. It also occurs due to regenerative load.



Voltage transient due to switching ckt with inductive load across i/p.

Overvoltage protection

In various sources of voltage transients it is almost necessary in a power semiconductor equipment to provide a means of limiting transient overvoltages which could otherwise overstress the semiconductor devices.

To protect against all sources of voltage transients, it is necessary to protect each device individually.

A simple means of protecting the devices against overvoltages is to introduce a safety factor V_p.

Inorder to keep the protective components to a min, devices are selected with their peak vol ratings of 1.5 to 2.5 times their normal peak working vol.

The effect of overvoltages is usually minimized by using the following protective elements & ckts.

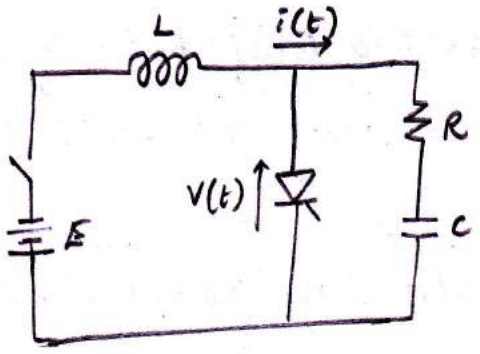
(i) snubber circuits (ii) Non-linear surge suppressors (iii) Crow-bar circuits.

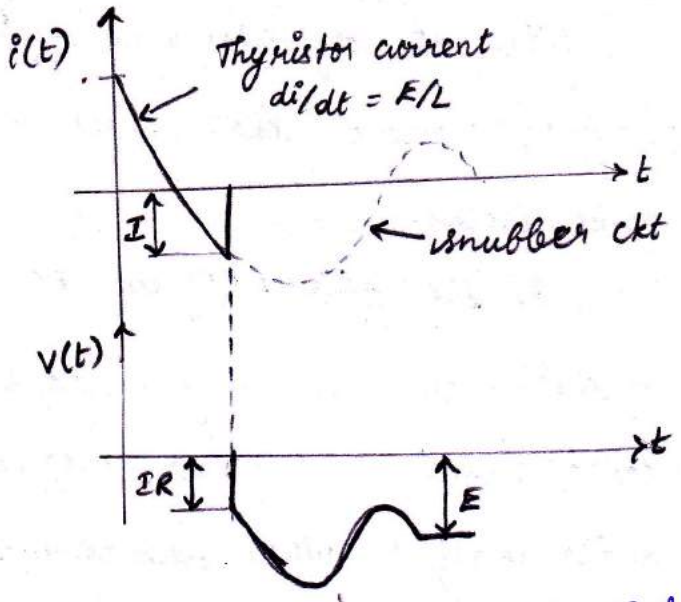
Snubber circuits (dv/dt suppression)

The tendency to excessive dv/dt may arise from external causes such as the closing of main supply contactor, or from the operation of the ckt itself.

dv/dt suppression is achieved by means of snubber ckt.

The snubber ckt basically consists of a series-connected resistor & capacitor placed in shunt with an SCR as shown in fig.





A capacitor C across the thyristor means that any high dv/dt appearing at the thyristor terminals will set up an appropriate current $\left(= C \frac{dv}{dt}\right)$ in the capacitor.

The inductance in the circuit will severely limit the magnitude of the current to the capacitor & hence limit dv/dt.

In fig, the inductance, L, is the effective ckt inductance & its presence limits the initial di/dt of the device at turn "on".

A series inductor, either linear or saturable, may be introduced to augment the supply ckt inductance.

Normally, the LCR ckt is slightly underdamped, & when a forward voltage step is applied to it, the peak voltage appearing across the device & its rate of change are both limited to acceptable values.

Snubber losses can be appreciable, particularly at high-switching frequencies.

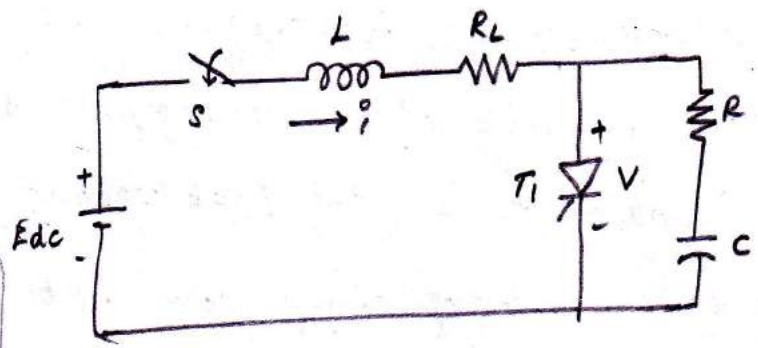
When the thyristor turn-off, there is a brief pulse of reverse recovery current that rises to a peak value, at which time the device blocks.

In the absence of an RC snubber, the abrupt interruption of the reverse recovery current in the series inductance, L, will cause transient $L\,di/dt$ overvoltages that may destroy the device itself or other semiconductors in the converter ckt.

When thyristor T_1 is turns-on, the snubber capacitor, C, discharges into the thyristor, but resistor R limits the discharge current & prevents excessive di/dt at turn on.

However, at turn off, a forward IR voltage drop suddenly appears across the thyristor due to reverse recovery of the diode. Thus the presence of the resistor impairs the forward dv/dt limiting performance of the snubber.

a) Design of snubber n/w for dc circuit.



when switch S is closed, the capacitor behaves like a short circuit & SCR in the fwd blocking state offers a very high resis.

The value of capacitor is given as $C = \frac{1}{2L}\left(\frac{0.564\,V_m}{dv/dt}\right)^2$

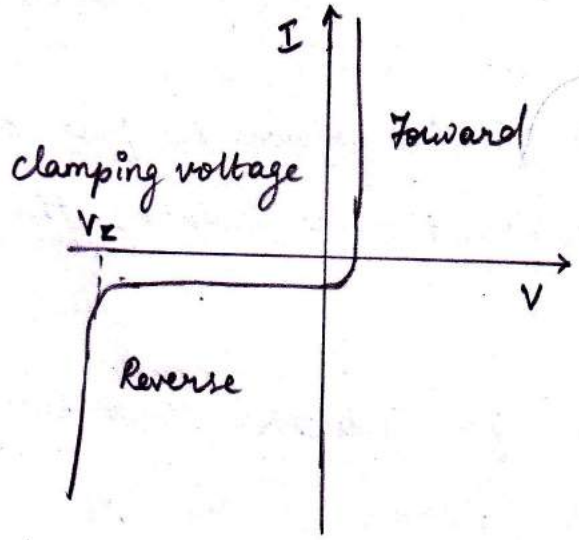
Where V_m → peak value of supply voltage.

dv/dt → the permissible dv/dt

L → source inductance.

And resistance is given as, $R = 2\sigma\sqrt{\frac{L}{C}}$ σ → damping factor.

Non-linear surge suppressors.

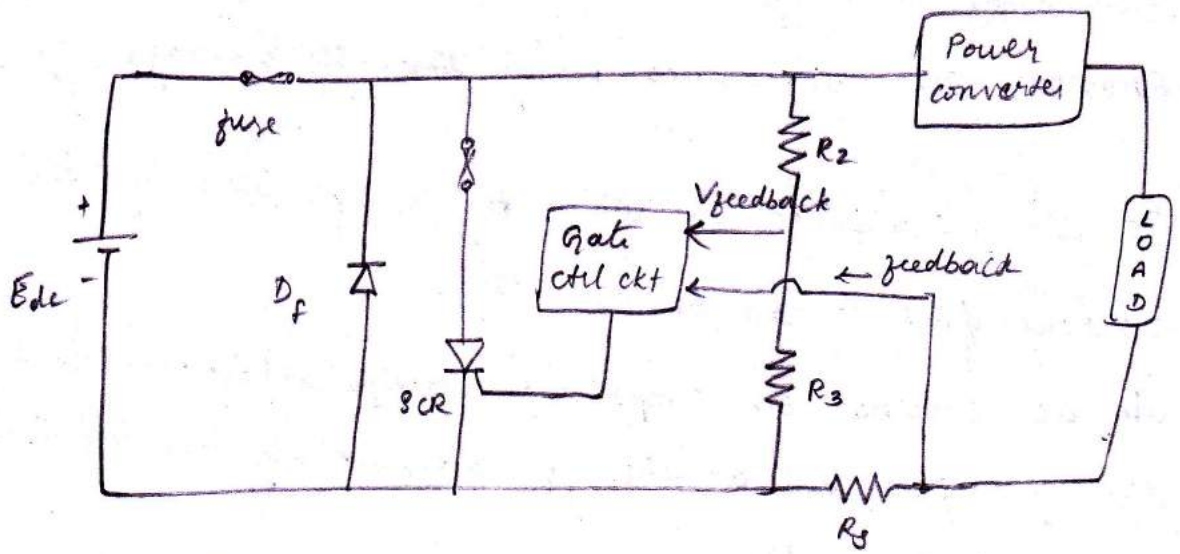


Non-linear devices having the kind of characteristics illustrated in fig are frequently used in place of, or in conjunction with, relative n/w's as a mean of limiting vol surges, being so selected that they pass an acceptably small ct at the normally working vol but a sufficiently large ct at higher voltages to limit surges at a tolerable level.

Devices of this kind are : (i) Varistors (ii) Selenium surge-suppressors.

Crowbar circuit

A crowbar can be used for overvoltage & / or overcurrent protection in both ac & dc circuits.



SCR Crowbar for overvoltage & overcurrent protection.

Whenever a fault condn occurs the crowbar SCR is triggered shorting the supply.

The resultant high-supply ckt flowing blows the fuse, or initiates a fast-acting ckt breaker, thereby isolating the load from the supply.

Diode D_f provides a ckt path for inductive load energy.

Load ckt is measured by the voltage across the sense resistor R.

When this voltage reaches a preset limit, that is the load ckt has reached the fault-level, the SCR is triggered.

The load or dc link voltage is measured from the resistor divider $R_2 - R_3$.

When this voltage exceeds the predetermined limit, the SCR is triggered & the fuse is blown by the crowbar short-circuit current, isolating the sensitive load from the supply.

Crowbar SCR can conduct many times its average ckt rating.

For the few millisec in which the fuse is isolating, the SCR's surge current feature can be exploited.

An ac crowbar can comprise two antiparallel-connected SCRs across the fuse-protected ac line, or alternatively one SCR in a four diode rectifying bridge.

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UNIT-V PROTECTION AND COOLING OF POWER SWITCHING DEVICES.

[MD Singh K.B. Khanchandani Pg: 516 – 540.

OVER CURRENT FAULT CONDITION

Most thyristor circuits are fast operating and can be controlled in such a way as to prevent the load current from rising too high to cause circuit damage or mal operation.

However, there are a number of component failures and circuit maloperation conditions where the current can rise out of control to many times the normal rated value and steps have to be taken to limit these conditions and to protect the other circuit components against the effect of the high current.

An overcurrent can occur due to any of the following causes.

(i) Output short-circuit
(ii) Internal faults in a thyristor circuit
(iii) Inversion failure in naturally commutated circuits
(iv) Commutation failure in a forced-commutation circuits and
(v) Short circuit between one of the phases of mains and the bridge.

(i) Output Short-circuits.

On any system, output short circuit can occur and in many situations gate control of the thyristor

cannot prevent high currents from flowing flowing, this will quickly result in loss of control of the thyristors due to over-temperature or commutation failure.

The maximum level of the fault current during short-circuit will occur at zero delay angle α and at specific instants of the short-circuit during the cycle.

$$\text{Steady-state fault current} = \frac{\text{Circuit voltage}}{\text{Circuit Impedance}}$$

If the fault causes large capacitors to be short-circuited, their discharge currents can further increase the circuit fault current.

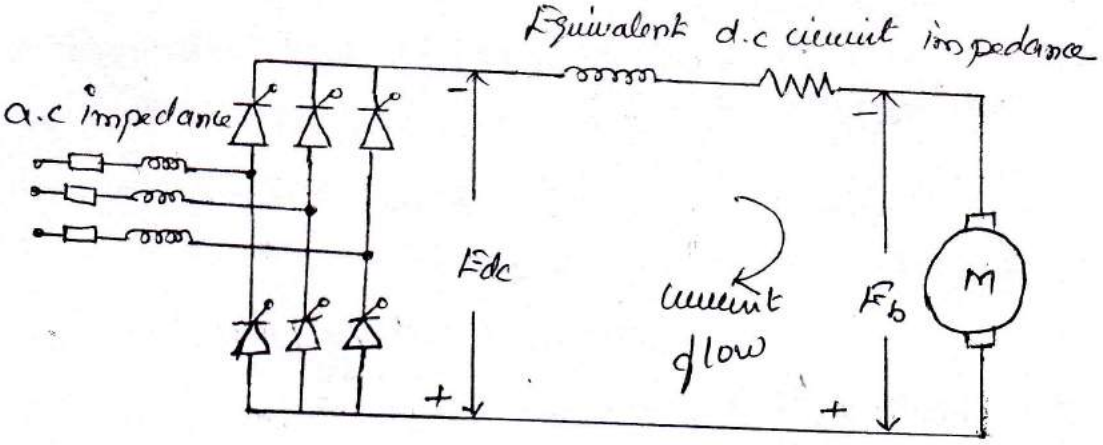
This is of particular importance in forced-commutated circuits where large filtering capacitors are used. Conversely, the presence of d.c. circuit inductance will slow up the rate of rise of fault current.

In naturally-commutated circuits, the output short-circuit current will also split-up between the thyristors of the circuit, and the effective overlap angles will be much larger than under normal operating conditions.

Steady-state fault currents in naturally commutated rectifier circuits.

Circuit	dc short circuit mean current	a.c. RMS short circuit current.	Thyristor Peak current	Thyristor Mean current	Half-cycle I^2t thyristor (Amp-sec^2)
1. Single Phase Half and fully controlled bridge	I_F	$\frac{\pi}{2\sqrt{2}} \cdot I_F$	$\frac{\pi}{2} I_F$	$\frac{1}{2} I_F$	$\frac{\pi^2}{8} 10^{-3} I$
2. Three phase Half and fully Controlled bridge	I_F	$\frac{\pi}{3\sqrt{2}} I_F$	$\frac{\pi}{3} I_F$	$\frac{1}{3} I_F$	$\frac{\pi^2}{18} 10^{-3} I$
3. Six phase half wave	I_F	$\frac{\pi}{6\sqrt{2}} \cdot I_F$	$\frac{\pi}{6} I_F$	$\frac{1}{6} \cdot I_F$	$\frac{\pi^2}{72} 10^{-3}$

the motor through the circuit impedance.



Inversion failure

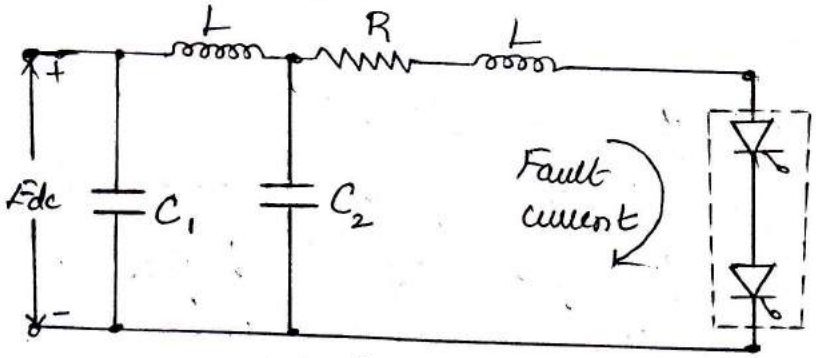
A higher fault condition may result from a firing or control circuit fault which causes the converter suddenly to switch into fully rectifying condition, in which case the total circuit voltage will be the sum of E_{dc} and E_b.

An intermediate condition occurs if all the firing pulses suddenly disappears as those thyristors in the circuit which are carrying current to that instant continue to do so. The total circuit voltage under these conditions will be single-phase of the supply voltage ie, a sinusoidally changing voltage, pulsed the motor voltage; the fault current will flow through both the a.c and d.c. circuits.

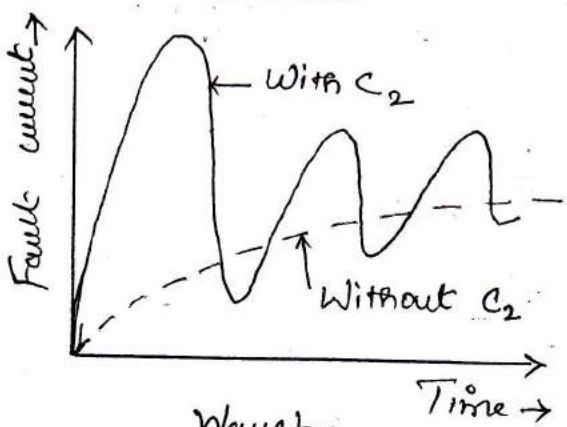
(iv) Commutation failure in forced commutation circuit.

Correct Operation of all forced commutation inverter circuits depends on the ability of the commutating components to provide sufficient time for the thyristors to

turn-off. If, due to excessive load-current, or insufficient charge on commutating capacitors, or incorrect firing of the thyristors, a thyristor does not have time to turn off, it will stay in the on-state, result in the d.c. supply being short-circuited by the thyristors.



circuit



Waveform

Fault current caused by Commutation failure

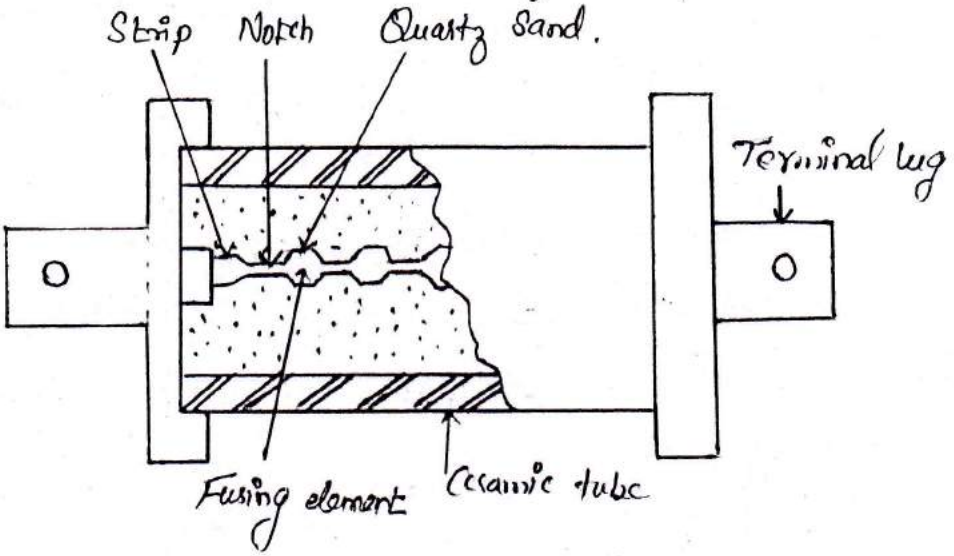
The fault current then flowing will depend on the circuit inductance, resistance and capacitance. The capacitance close to the inverter circuit will cause an initial high discharge current through the thyristors limited only by the local resistance and inductance near to the thyristors. An inductive input circuit ie, significant L and no C_2, will result in a comparatively slow build-up of fault current.

If the inverter has more phases and thyristors, other conditions of commutation failure may be possible but they will all result in either the full d.c. short-circuit current flowing through an individual thyristor or it will be shared with the other phases.

OVER CURRENT PROTECTION.

As the fault current increases, the fuse operates and clears the fault current in few milliseconds.

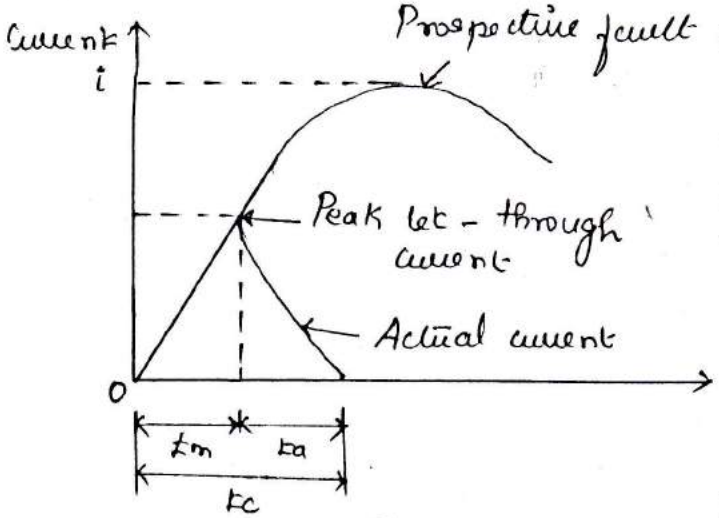
In general, the fuse consists of (i) fusing element (ii) ceramic-tube and (iii) lugs.



Fuse link-geometry [Semiconductor fuse and its cross section]

The fusing element is made of silver with one or more necks. The body of the fuse is made of ceramic material. The large contact blade or legs facilitate connection and dissipate heat.

The fusing element is embedded in a special sand which can conduct heat and serve as a quenching medium for the arc at the time of fusing.

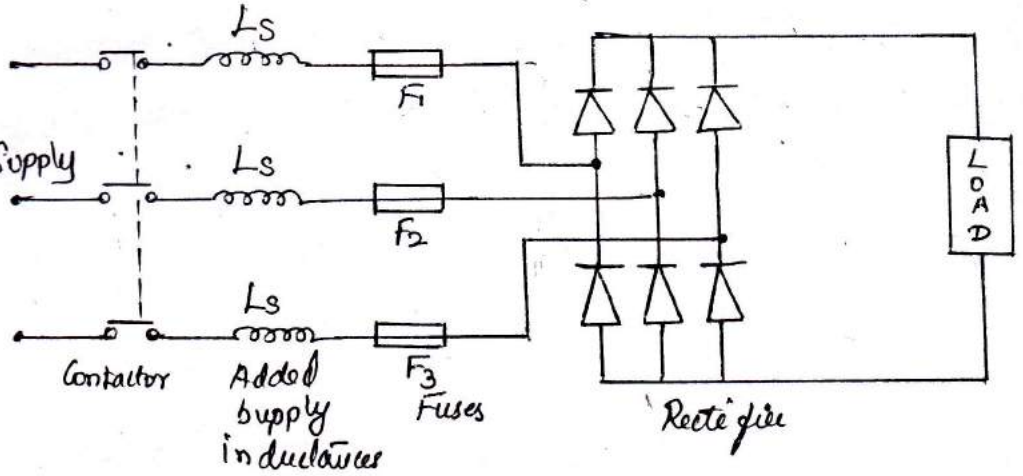


Fuse current.

The clearing time t_c is the sum of melting time t_m and arc time t_a. t_m is dependent on load current, whereas t_a is dependent on the power-factor or parameters of the fault-circuit.

The fault is normally cleared before the fault current reaches its first peak, and the fault current, which might have blown if there was no fuse, is called the prospective fault current.

In general, larger the equipment rating, the more tendency is there to fuse the devices individually. It may necessary to add inductance to limit the rate of rise of the fault current and hence avoid excessive stress on the fuse and device.



Positioning of fuses and added inductors for Passive l

However, this inductance may affect the normal performance of the converter.

(i) Fuse - SCR Co-ordination in A.C. Circuits.

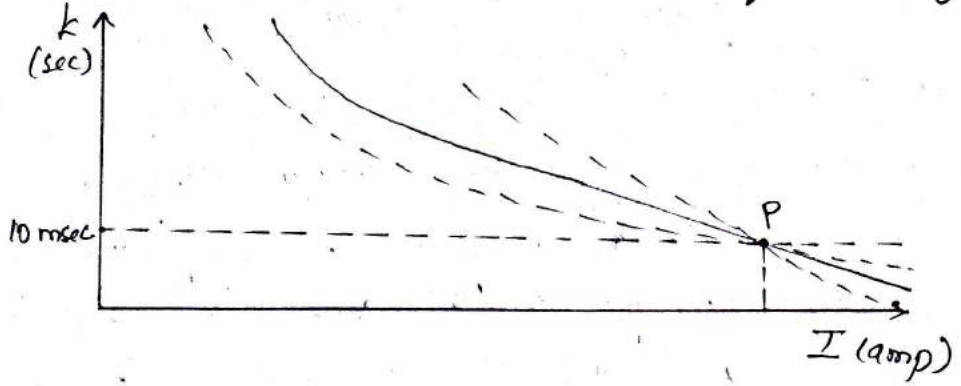
A fast acting fuse can be used for protecting thyristors against large surge currents of very short duration called subcycle surge currents.

The coordination of the fusing time with the subcycle duration rating of the device is essential. The one cycle surge rating $\hat{I}$ of an SCR is defined as the peak amplitude of the sinusoidal current which the SCR can carry for one half-cycle (10 ms on a 50 Hz basis).

The subcycle - surge current rating may be obtained from

$$\hat{I}_{\text{subcycle (t)}} = \sqrt{\frac{\hat{I}^2 \times 1/100}{t}}$$

where $\hat{I}_{subcycle}(t)$ is the peak amplitude of the sinusoidal whose period is $2t$ and t is the duration of the surge in seconds



Fuse and circuit breaker coordination.

Assuming that the fault current waveform is triangular, the fusing time t_c will be

$$t_c = \frac{3 \cdot I_k^2}{I_p^2}$$

where I_p is the peak magnitude of the let-through fault current.

The fuse will provide protection when the current is higher than that corresponding to point P. For lower-currents, the device will usually be protected by the circuit-breaker.

(ii) Fuses in D.C Circuits.

Fuse protection in d.c circuits presents greater problems than in a.c. circuits.

Since natural periodic current zeros do not occur, there is no equivalent to the long-term current/time characteristics for fuses, and moderate or slowly rising fault-currents can produce a dangerous condition by allowing the fuse to arc

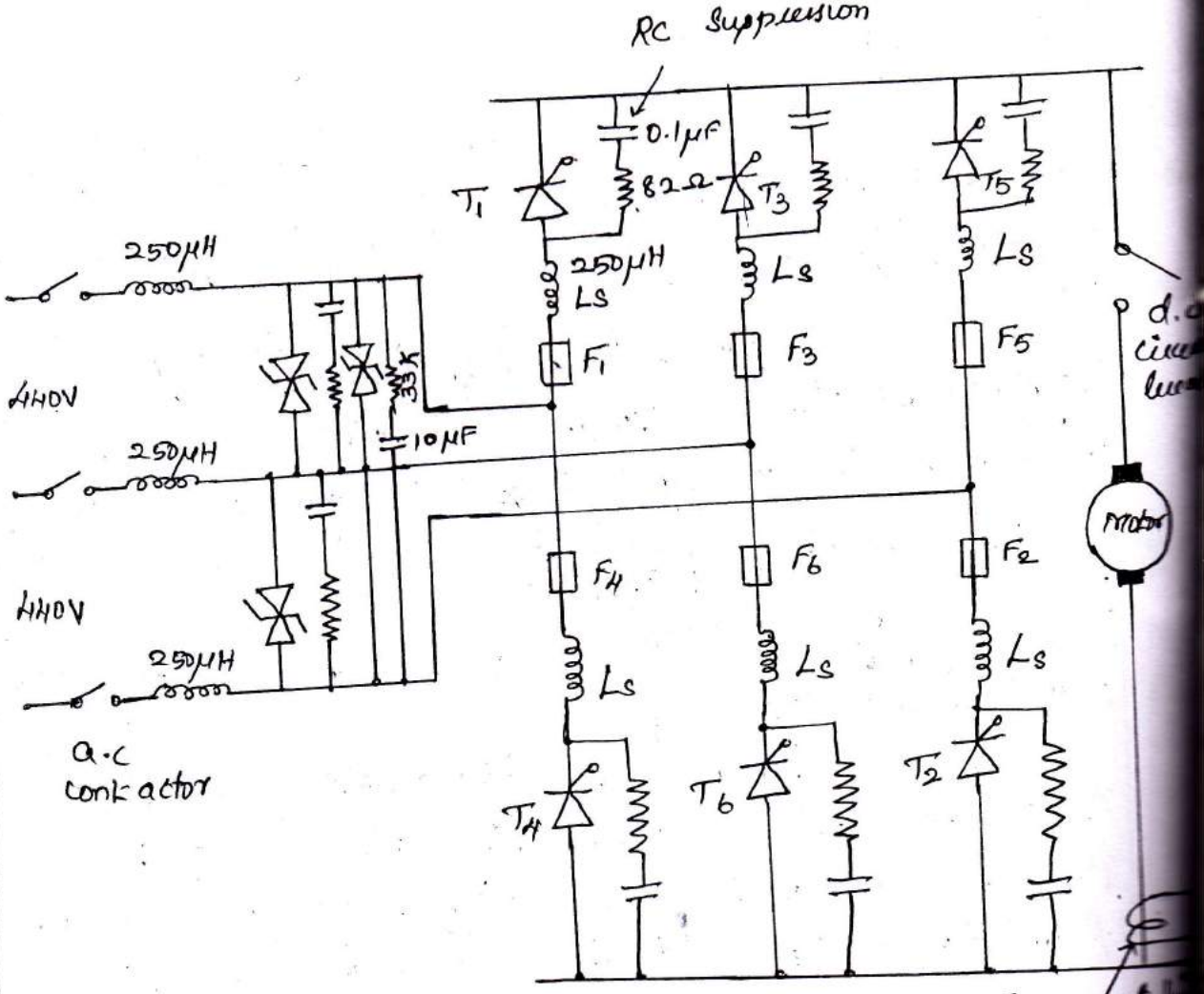
continuously without breaking the current.

The use of fuses in d.c circuit is therefore subject to important restrictions regarding minimum prosp fault current, the maximum circuit time constant (L/R) und fault conditions, and the supply voltage.

It is therefore necessary to have separate d peak let-through current values in relation to the fuse clearing time in order to coordinate with the SCR's surge capability.

(iii) Complete Protection of Converter.

The following circuit shows elements giving comp protection to surge currents and voltages, dv/dt and di/dt and the contractors for the long-time low level overload.



Complete Protection of a Converter.

To current
via

GATE PROTECTION.

(i) Radio Interference Phenomenon.

The induced voltages may turn on the thyristors at wrong instances, causing mal operation of the entire control scheme. This phenomenon is known as radio interference phenomenon.

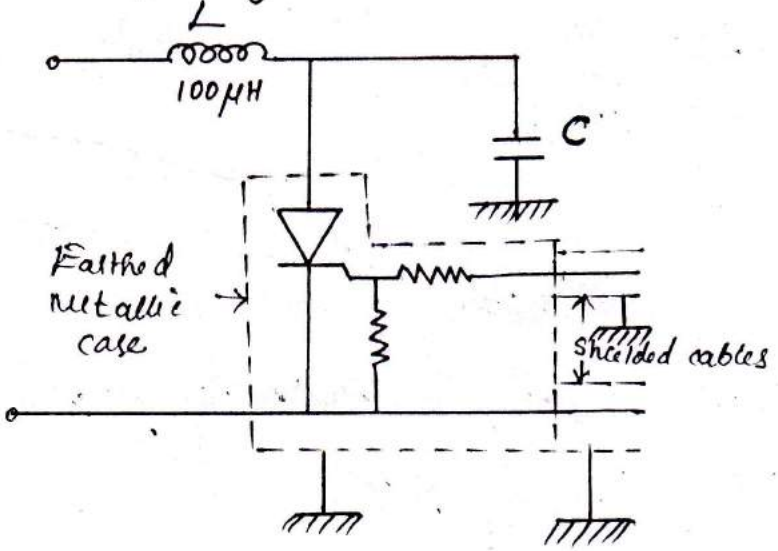
The effect of radio interference phenomenon is usually minimized by using the following elements and circuits.

(i) Shielding
(ii) R-F filter
(iii) Zero-voltage switching.
(iv) Use of Snubber
(v) Other Precautive Measures.

(i) Shielding.

The interference by external electric and magnetic fields induces spurious signals in the gate to cathode circuit.

Hence it is very important to protect the gate control by using shielded cables.



R-F Filter and Shielding.

Generally, the radiated noise is effectively shielded by the metal cabinets used for housing the power electronic equipment.

Additional steps may be necessary if the power electronic equipment is operating near sensitive communication or medical equipment.

(iii) R-F Filters:

The filter consists of a small inductance which is connected in series of the SCR and shunt capacitor. Inductor slows down the rate of change of forward current and capacitor reduces the rate of decay of the forward-voltage.

$$X_L = R_L = X_C$$

where R_L is the load-resistance.

Now, for a radio-frequency band, the values of L and C will be,

$$2\pi f_0 L = R_L = \frac{1}{2\pi f_0 C}$$

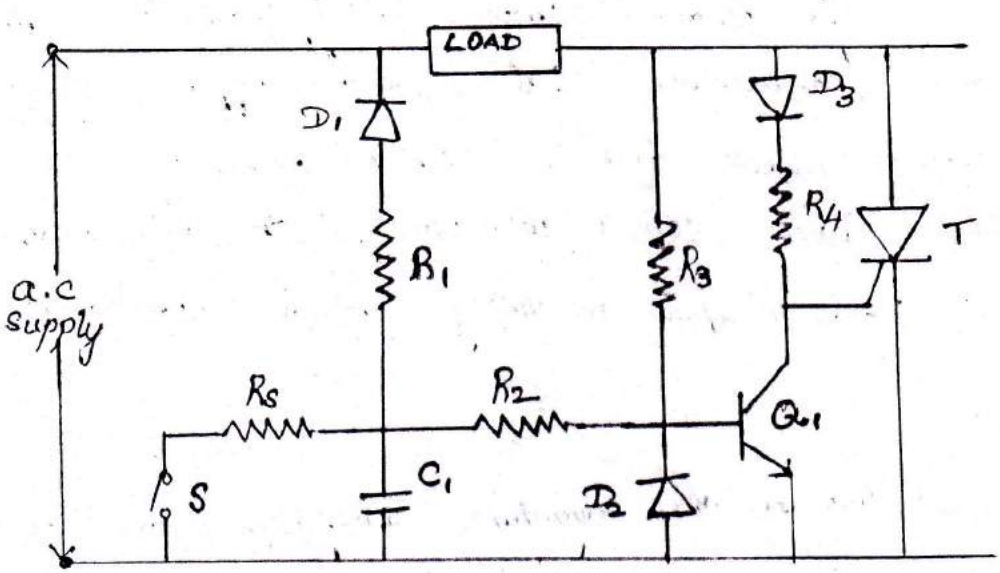
$$L = \frac{R_L}{2\pi f_0}$$

and $$C = \frac{1}{2\pi R_L \cdot f_0}$$

where f_0 is the corner or breakpoint frequency, usually taken as 50 kHz, for the filter.

(iii) Zero - Voltage Switching.

By eliminating the sudden steps of current, the RF noise contribution is brought to an absolute minimum. This eliminates the need for RF filter components which for longer heating load, can become quite large and costly.



Ideal half - wave zero voltage switch.

Circuit Operation.

The ON-OFF action of thyristor T_1 depends upon the state of transistor Q_1 and the state of transistor Q_1 is controlled by the switch S.

When transistor Q_1 is cut-off, positive anode voltage on SCR T_1 causes the gate current to flow through D_3 and R_4, triggering SCR T_1 into conduction.

When transistor Q_1 is biased into conduction, the

current through R_4 is shunted away from the gate of SCR T_1 through the collector of Q_1.

Mode 1 :

Consider the positive half-cycle and switch S clos The supply current has the first path, L-Load $-R_3-R_2-R_5-N$ This current causes a potential drop across R_3, R_2 and R_5.

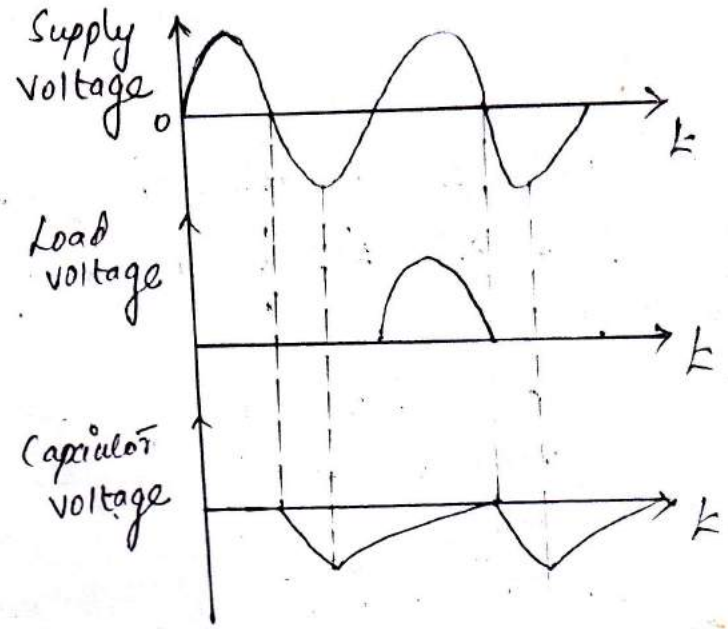
This potential drop is sufficient to drive transis Q_1 in the saturation state, which offers negligible resista The supply current has the second path, L-Load $-D_3-R_4-$

Hence, SCR T_1 will not get the gate pulse and becomes off. Therefore, no voltage will be applied to the load.

Mode 2 :

Consider the negative half-cycle and switch S opened. With this condition, Capacitor C_1 will charge to the peak of the supply voltage through R_1 and D_1.

The charging path becomes $N-G_+-C_1-R_1-D_1-L$.



Load and Capacitor Voltage Waveform.

As the a.c supply voltage drops from its negative peak, capacitor C_1 discharges through D_2 and R_2.

This makes diode D_2 forward biased and this diode applies negative bias to transistor Q_1.

When switch S is closed, SCR T_1 will stop conducting at the end of the present or previous positive half-cycle and will not get triggered again.

Similarly, when switch S is opened, SCR T_1 will be turned-ON, only at the beginning of positive half-cycle of the applied-voltage.

(iv) Use of Snubber.

From the point of view of EMI reduction, a properly designed snubber is quite effectively, since it reduces both the dV/dt and di/dt of the circuit.

(v) Other Preventive Measures.

All current carrying conductors should be run in close proximity to the return wire, such as by copper strips. A twisted pair of wires will reduce the generated external field to a minimum.

To reduce the stray capacitances, the area of exposed metal at the switching potential should be minimize and kept as far from the ground as possible by proper mechanical design.

HEAT SINKS.

(i) Temperature control in semiconductor devices
(ii) Heat Transfer.

(iii) Thermal Resistance and Thermal model.
(iv) Transient Thermal Impedance
(v) Heat sink Specification

Power dissipation in electrical components causes the internal temperature and affects performance and reliability.

(i) Temperature control in Semiconductor Devices.

The p-n junction would lose rectifying property at this limit temperature.

The maximum allowed temperature is far below this theoretical limit manufacturers specify a maximum temperature, known as maximum junction temperature T_j.

This is also known as the worst-case temperature in the design procedure. Typical semiconductor packages are designed for $T_{j\,max}$ of 125°C.

(ii) Heat Transfer.

Heat transfer takes place in 3 ways.
a) conduction,
b) convection and
c) Radiation.

Conduction is the heat transfer among stationary interfaces by the vibratory motion of atoms or molecules.

Convection is the mechanical transport of heat by a moving fluid or gas.

Heat energy is converted into electromagnetic radiation in heat transfer by radiation which is

absorbed by other components in the vicinity.

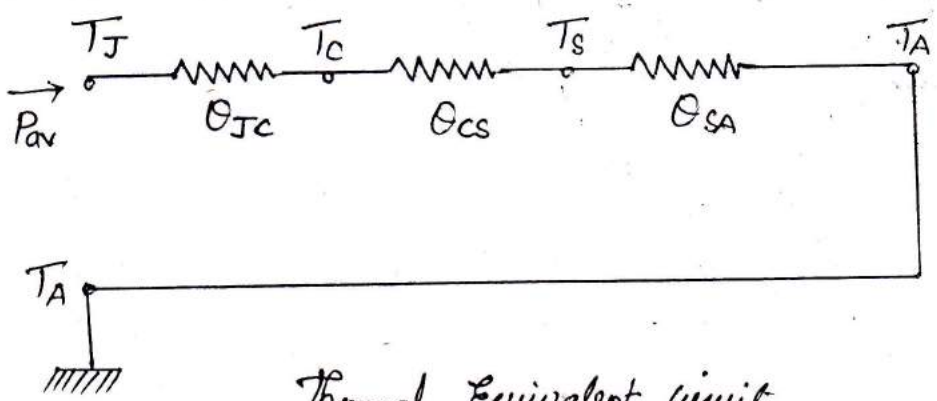
The heat transfer in power-electronic systems is dominated by conduction and convection processes.

(iii) Thermal Resistance and Thermal Model.

Thermal energy flow takes place from a region of high temperature to a region of lower temperature.

By analogy with Ohm's Law, the steady-state temperature difference $(T_1 - T_2)$ when a constant thermal power of P_{av} watts flows through a thermal resistance θ_{12} °C/W is given by

$$\theta_{12} = \frac{T_1 - T_2}{P_{av}} \quad °C/W, \quad T_1 > T_2.$$



Thermal Equivalent circuit

The steady-state temperature difference between junction and ambient is given by

$$T_J - T_A = P_{av}(\theta_{JC} + \theta_{CS} + \theta_{SA})$$

Where

θ_{JC} - thermal resistance from junction to case, °C/W

θ_{CS} - thermal resistance from case to sink, °C/W.

θ_{SA} - thermal resistance from sink to ambient, °C/

Also,

$$P = \frac{T_J - T_C}{\theta_{JC}} = \frac{T_C - T_S}{\theta_{CS}} = \frac{T_S - T_A}{\theta_{SA}} = \frac{T_J - T_A}{\theta_{JA}}$$

where $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$, the total thermal resistance between junction and ambient.

(iv) Transient Thermal Impedance.

The thermal resistance of the static model changes to the thermal impedance, which includes heat capacity.

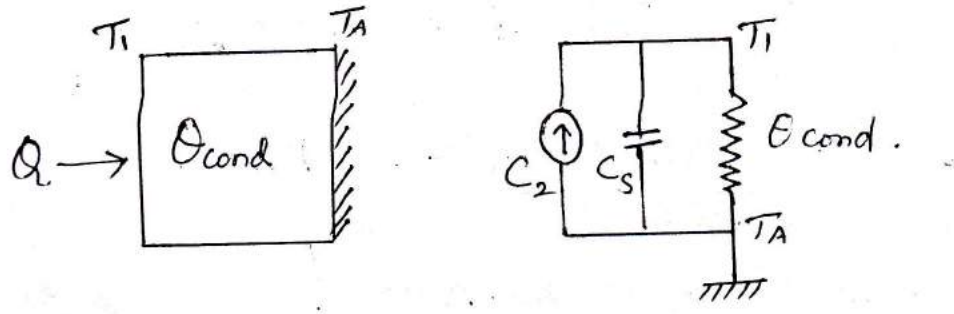
The heat capacity C_S is defined as the amount of heat (energy) stored in a unit mass that would rise its temperature by a unit degree.

$$C_S = \frac{dH}{dt}$$

where $dH = Q \cdot dt$.

$$\Rightarrow Q = \frac{dH}{dt}.$$

$\therefore$ Thermal Power, $Q = C_S \cdot \frac{dT_A}{dt}$.

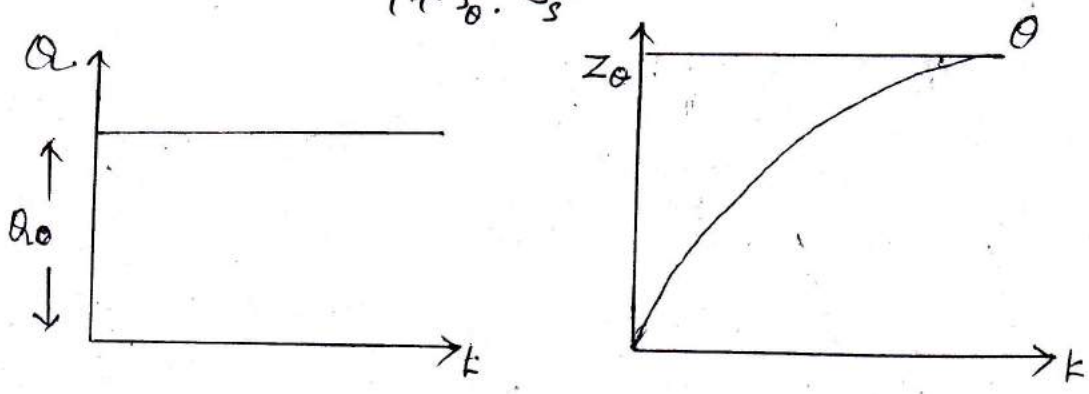


Thermal Equivalent circuit in Transient heat Transfer.

Thermal Impedance using Laplace - transform is

$$T_i = Z_\theta \cdot Q$$

where $Z_\theta = \dfrac{\theta}{1 + s_\theta \cdot C_s}$



Transient thermal impedance.

For a step - change in the amount of heat imparted, upon application of a step power input Q_0, the steady - state rise in the temperature is given by

$$T_{1,ss} = T_{1,0} + \theta \cdot Q_0.$$

The instantaneous temperature follows an exponential path,

$$T_i = T_{1,0} + \theta \cdot Q_0 (1 - e^{-t/\tau})$$

where $\tau = \theta \cdot C_s$.

Rearranging the variables in the above equation,

$$T_i = T_{1,0} + Z_{\theta(t)} - Q_0$$

and

$$Z_\theta = \theta \cdot (1 - e^{-t/\tau})$$

Impedance Z_θ can be said to be an exponential function of time.

(v) Heat - Sink Specifications.

The thyristor data sheet specifies the maximum allowable junction temperature, $T_{J(max)}$ and θ_{JC}.

The continuous d.c. current rating of the device can be evaluated with the use of the on-state voltage current characteristic.

Conversely, if the heat-sink has been specified, the junction temperature can be determined for a given on-state current and ambient temperature.

Neglecting θ_{CS}, the heat-sink thermal resistance is given by,

$$\theta_{SA} = \frac{T_C - T_A}{P_{AV}}$$

The average power dissipation permitted is less than the steady-state d.c. power dissipation. This derating is necessary because the instantaneous junction temperature varies cyclically above and below the average value due to the pulsating nature of the power loss.

Consequently, the average junction temperature may be reduced if the peak allowable junction temperature exceeds average temperature by 5°C or more.

THYRISTOR MOUNTING CIRCUITS.

The internal power losses in a thyristor cause high thermal stresses which further give rise to mechanical forces.

Therefore, a thyristor must be braced to withstand such mechanical forces. In addition, the SCR mounting must be so designed as to facilitate heat flow from junction to the case.

(i) Lead Mounting
(ii) Stud Mounting
(iii) Bolt-down Mounting
(iv) Press-fit Mounting
(v) Pressure Mounting.

(i) Lead Mounting.

For load current rating of about one-ampere, lead mounted SCR are used. Such SCRs do not require any additional cooling or heat-sink. Their housings dissipate sufficient heat by radiation and convection.

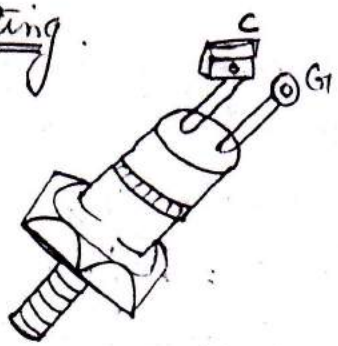
Lead Mounting

(ii) Stud Mounting.

The Stud mounted SCR is a flexible component and has wide acceptance.

This type of SCR uses a copper or aluminium stud with a machine thread for making mechanical electrical and thermal contact to a heat exchanger of the user's choice.

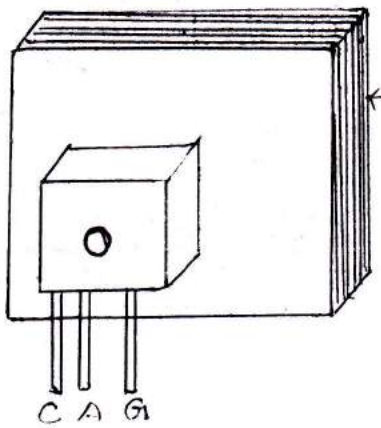
Stud Mounting.



The threaded stud can have different sizes. The SCR is attached to heat-sink by means of threaded stud and nut. Their anode gets electrically connected to the heat sink.

This method of mounting is common with small or medium sized thyristors.

(iii) Bolt-down Mounting.



The device has flanges or tabs which usually contain one or more holes.

Bolts are placed through these holes in order to attach the device to the heat-sink.

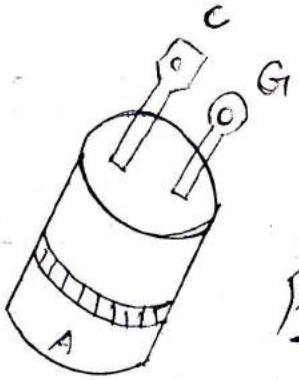
This type of mounting is common in medium and small ratings.

This is also called as flat pack mounting.

(iv) Press-fit Mounting.

This package is designed primarily for forced insertion into a slightly undersized hole in the heat-exchanger.

When properly mounted, this type of SCR has a lower-thermal drop to the heat exchanger than the stud type mounting.



Press-fit Mounting

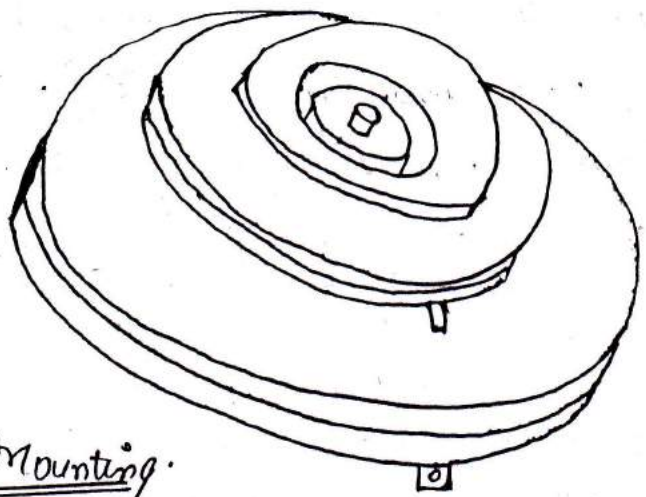
Also in high volume applications the cost of this type of mounting is generally less than that for the stud-type of SCR. This type of mounting is employed for thyristors of a large rating.

(v) Pressure Mounting.

This device is clamped under a very large external force.

Such devices are also called Hockey-puk SCRs because of their shape.

The clamping force is applied smoothly, evenly and perpendicularly to Hockey-puk to insure that there is no deformation to either the pole faces or the heat-exchangers during mounting.



Pressure Mounting.

It is possible to have double side cooling using air cooled or liquid cooled heat exchangers.

This type of mounting is used for thyristors of very high-current ratings.

12E605 POWER ELECTRONICS

3 1 0 3.5

OBJECTIVES:

- To realize the construction and performance of power semiconductor devices.
- To illustrate the switching characteristics of power semiconductor devices.
- To recognize the operational behaviour of controlled rectifiers and DC choppers.
- To impart the concepts of inverters and cycloconverters.
- To categorize various protection and cooling methods of power semiconductor devices.

OUTCOMES:

Learners should be able to

- familiarize with the fundamental concepts and characteristics of various power semiconductor devices.
- understand and analyze the controlled rectifiers, choppers, inverters and cycloconverters.
- get an exposure to various protection and cooling methods of power semiconductor devices.

UNIT I POWER SEMICONDUCTOR DEVICES 9

Structure, operation and characteristics of SCR, TRIAC, power transistor, MOSFET, IGBT, IGCT and GTO – Switching characteristics of SCR, power transistor, MOSFET, IGBT and GTO – Gate triggering circuit.

UNIT II CONTROLLED RECTIFIERS [QUALITATIVE STUDY ONLY] 9

Single phase half controlled and fully controlled thyristor bridge converters: circuit operation, estimation of average, RMS load voltage and load current for continuous current operation for R, RL, RLE loads – Three phase half and fully controlled thyristor converters for R, RL and RLE loads – Dual converters.

UNIT III CHOPPERS AND ITS APPLICATIONS 9

Introduction – Operation of step-up and step-down choppers – Time ratio control and current limit control – Switching mode regulators: buck, boost, buck-boost and cuk converters.

UNIT IV INVERTERS AND CYCLOCONVERTER 9

Single phase and three phase (both 120^0 mode and 180^0 mode) inverters – Voltage and harmonic control – PWM techniques: sinusoidal PWM, modified sinusoidal PWM and multiple PWM – Series resonant inverter – Current source inverters – Cycloconverters (single phase to single phase, three phase to single phase) – AC voltage controllers.

UNIT V PROTECTION AND COOLING OF POWER SWITCHING DEVICES 9

Introduction – Over voltage condition and protection: naturally commutated circuits and forced commutated circuits – Over current fault condition and protection – Gate protection – Thyristor mounting circuits – Heat sinks.

TOTAL: 45 + 15

TEXT BOOKS:

Sl. No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Singh M D Khanchandani L	Power Electronics	Tata McGraw Hill, Second Edition (Third Reprint)	2008
2.	Bimbhra P S	Power Electronics	Khanna Publishers, New Delhi.	2012

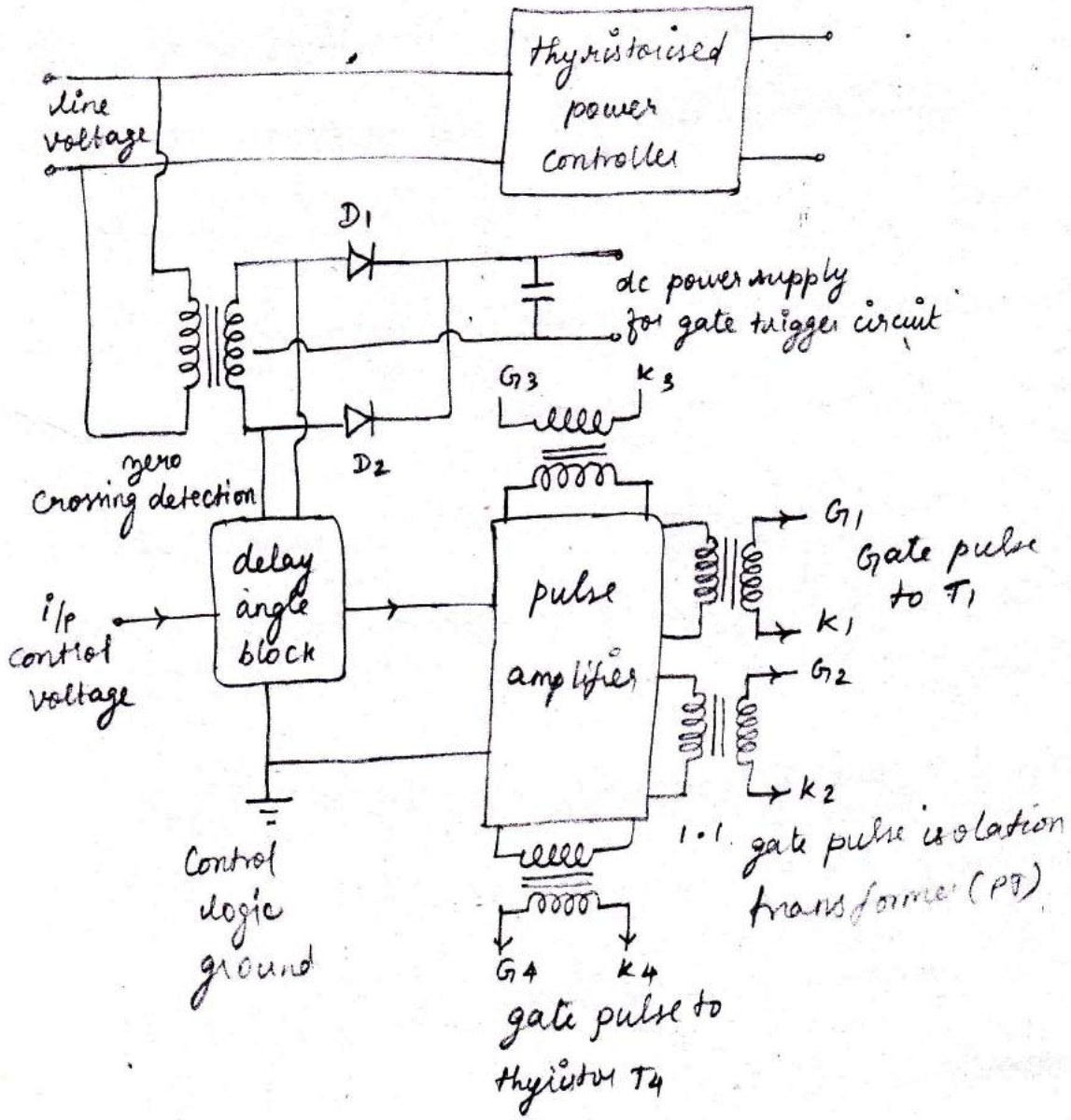
REFERENCE BOOKS:

Sl. No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Rashid M H	Power Electronics – Circuits, Devices and Applications	Pearson Education (Singapore) Pvt. Ltd	2013
2.	Ned Mohan Undeland Robbins	Power Electronics - Converters, Applications and Design	John Wiley and sons (Asia)	2009
3.	Vedam Subrahmanyam	Power Electronics	New Age International (P) Limited	2004
4.	Philip T Krein	Elements of Power Electronics	Oxford University Press, Inc	2005

WEB URLs:

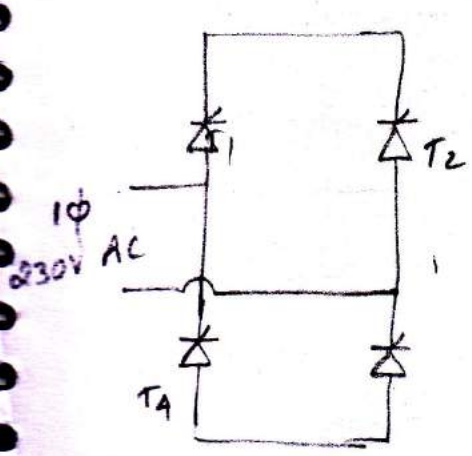
1. http://www.iitm.ac.in/nptel
2. http://www.services.eng.uts.edu.au
3. http://ocw.mit.edu/courses/electrical-engineering-and-computer-science
4. http://forum.jntuworld.com/showthread.php

ii) Draw & explain the gate triggering circuit for power semiconductor devices.



— (3m)

General Block diagram



The above fig shows the general block diagram of a gate-trig circuit.

The thyristors are at line potential & the trigger circuit must be referenced within respect to a logic ground associated with control i/p

The Zero cross detector & the gate pulse generated with zero crossing of the line voltage, must be isolated by means of transformers.

The dc voltage can be supplied by rectifying the o/p of the line voltage synchronization transformer.

The ac synchronization voltage is converted to ramp voltage in the delay angle block, which gets synchronised to the zero crossing of the line voltage.

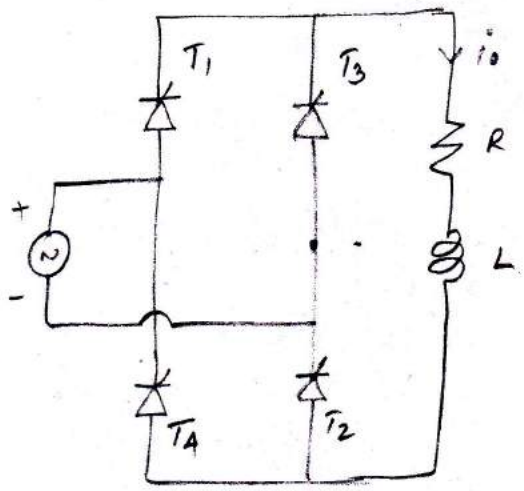
The ramp voltage is compared with control voltage.

By comparing this, the delay angle can be varied over nearly the full range between 0-180° & the delay angle is proportional to control voltage.

— (4m)

a) Derive the average o/p voltage equation, o/p current & RMS
ii) o/p voltage for 1φ full bridge controlled converter with RL load with its circuit diagram.

Circuit diagram:



(1m)

Average o/p voltage

$$V_o = \frac{1}{T}\int_0^T V_o(\omega t)\, d\omega t$$

$$= \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_m \sin\omega t \; d\omega t.$$

$$= \frac{V_m}{\pi}\int_{\alpha}^{\pi+\alpha} \sin\omega t \; d\omega t.$$

$$= \frac{V_m}{\pi}\left[-\cos\omega t\right]_{\alpha}^{\pi+\alpha}$$

$$= \frac{V_m}{\pi}\left[\cos(\pi+\alpha) + \cos\alpha\right]$$

$$= \frac{V_m}{\pi}\left[(-\cos\alpha) + \cos\alpha\right]$$

$$\boxed{V_o = \frac{2V_m}{\pi}\cos\alpha}$$

(2m)

Output current

$$I_o = \frac{V_o}{R}$$

$$= \frac{\frac{2V_m}{\pi}\cos\alpha}{R} \Rightarrow I_o = \frac{2V_m}{\pi R}\cos\alpha$$

(2m)

Average RMS voltage :

$$V_{o(rms)} = \left[\frac{1}{T} \int_0^T V_o^2(\omega t)\, d\omega t \right]^{1/2}$$

$$= \left[\frac{1}{\pi} \int_{\alpha}^{\pi+\alpha} (V_m \sin \omega t)^2 \, d\omega t \right]^{1/2}$$

$$= \left[\frac{V_m^2}{\pi} \int_{\alpha}^{\pi+\alpha} \frac{1 - \cos 2\omega t}{2} \, d\omega t \right]^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} \left[\omega t - \frac{\sin 2\omega t}{2} \right]_{\alpha}^{\pi+\alpha} \right\}^{1/2}$$

$$= \left\{ \frac{V_m^2}{2\pi} \left[\pi + \alpha - \frac{\sin 2(\pi+\alpha)}{2} - \alpha + \frac{\sin 2\alpha}{2} \right] \right\}$$

$$= \left\{ \frac{V_m^2}{2\pi} (\pi) \right\}^{1/2}$$

$$\boxed{V_{o(rms)} = \frac{V_m}{\sqrt{2}}}$$

$$\boxed{V_{o(rms)} = V_s.}$$

(2m)

The rms value of load voltage is same as rms value the AC supply voltage.

KARPAGAM COLLEGE OF ENGINEERING, COIMBATORE

CONTINUOUS INTERNAL ASSESSMENT - I

12E605 - POWER ELECTRONICS

ANSWER KEY

PART - A Answer All questions.

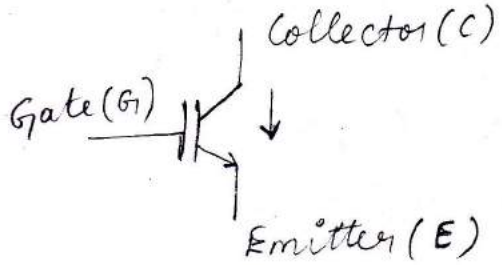
1. Define Latching current of SCR.

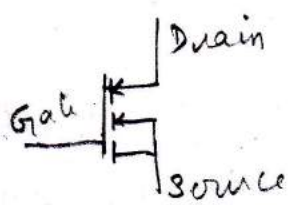
Latching current is the minimum forward current that flows through the SCR to keep it in forward conduction mode at the time of triggering. If forward current is less than latching current, SCR doesnot turn-on.

What is the four modes of operation of TRIAC.

Forward blocking mode
Forward conduction mode
Reverse blocking mode
Reverse conduction mode.

Draw the symbol of IGBT.





A4. Power MOSFET is a voltage controlled device. Why?

The power MOSFET is a voltage controlled device because its o/p characteristics determined by the field which depends on the voltage applied to gate & source of this MOSFET requires only small i/p current.

A5. Compare transistor with thyristor.

Transistor	Thyristor.
* made of 3 alternating semi-conductor layers (PNP or NPN)	* made of 4 alternating semiconductor layers (PNPN)
* Consists of two PN junctions	* consists of 3 PN junctions
* Consists of 3 terminals collector, emitter & base	* Consists of 3 terminals Anode, Cathode & gate
* Can not operate at higher voltages & current than thyristors	* can operate at higher voltages & current than transistors.
* Power handling is poorer than thyristor. [transistor power range is in watts]	* Power handling is better for thyristors because their ratings are given in kilowatts.

[any 4] — 2m.

What is meant by phase controlled rectifier?

The phase controlled rectifier converts the fixed AC voltage into controllable dc o/p voltage.

To obtain controllable o/p voltage thyristors are used instead of diodes. The o/p voltage of thyristor rectifiers is varied by controlling the delay (or) firing angle of thyristors.

Mention four applications of controlled rectifier.

The Controlled rectifiers are used in

battery chargers
DC power supplies
Speed control of dc drives.
HVDC transmission
DC traction drives, etc.,

any (4) - 2m.

What is the function of freewheeling diode in controlled rectifier?

It avoids the flow of current from load to source.
[∵ the energy stored in the load inductance is fedback to load itself in freewheeling action]
It avoids the o/p voltage being negative.
It avoids negative excursion (or) swing

any (2) - 2m.

Give an expression for average voltage for 1φ semiconverter with R and RL load.

R Load

$$V_o = \frac{V_m}{\pi}(1+\cos\alpha)$$

RL Load

$$V_o = \frac{V_m}{\pi}(1+\cos\alpha)$$

∵ The voltage waveforms for both R & RL load are same, the average voltage & RMS value of o/p voltage are also same.

A10. What is meant by ph delay angle of phase controlled rectifier?

The delay angle is the angle at which thyristors are triggered after zero crossing. After zero crossing of supply voltage, one pair of thyristors is forward biased.

After delay angle (α), these SCRs are triggered.

A8. What is the function of freewheeling diode in controlled rectifier?

When the load is inductive, the load current circulates through freewheeling diode

This freewheeling action avoids the flow of current from load to source.

Part - B.

2)

Draw and explain the VI characteristics of SCR.

The SCR characteristics can be obtained in 3 modes.

1) Reverse blocking mode
2) Forward blocking mode
3) Forward conduction mode.

The anode to cathode current I_{AK} is plotted with respect to anode to cathode voltage V_{AK}.

V_{BO} → Forward breakover voltage

V_{BR} → Reverse breakdown voltage.

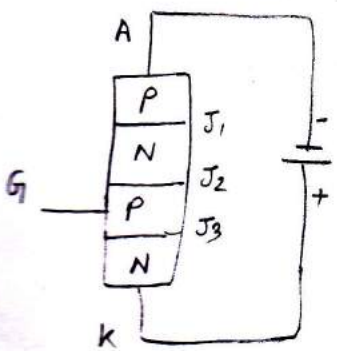
I_{g1}, I_{g2}, I_{g3} → gate current applied to SCR.

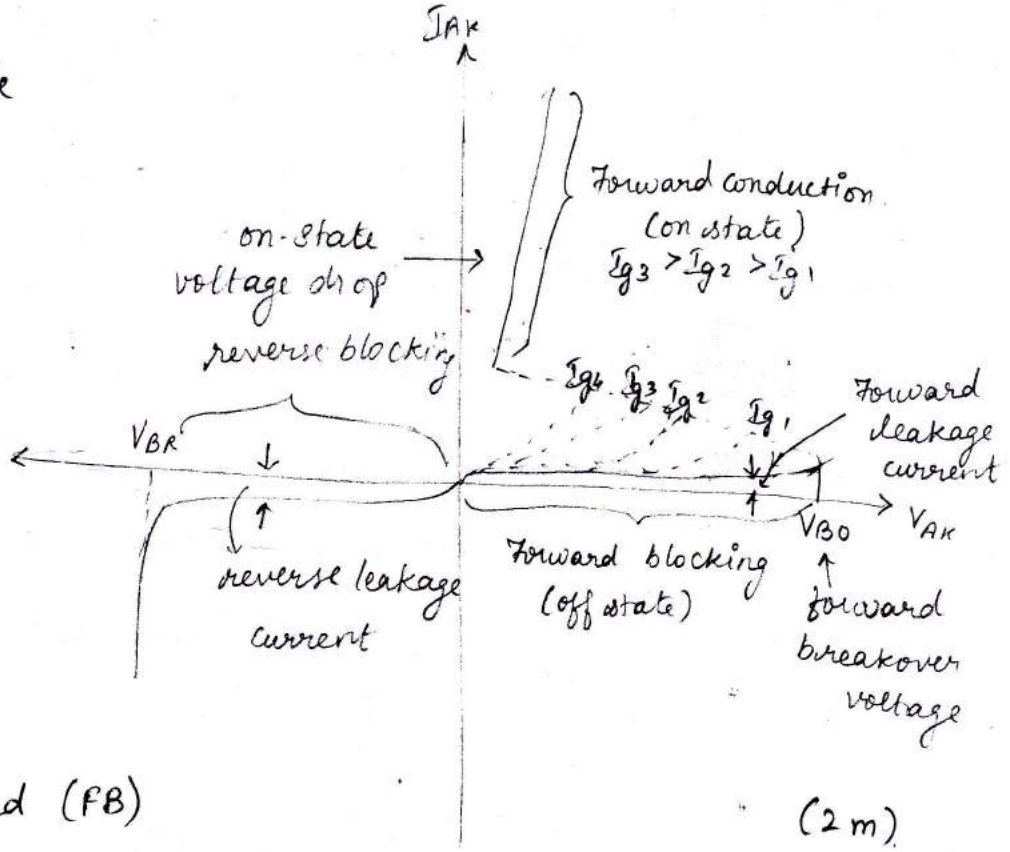
Reverse blocking mode

Anode - negative

Cathode - positive

gate - open.





J_2 - Forward biased (FB)

J_1 & J_3 - Reverse biased (RB)

SCR doesnot conduct in R_B.

Small leakage called reverse leakage current flows.

(2 m)

The above fig shows the reverse characteristics of SCR.

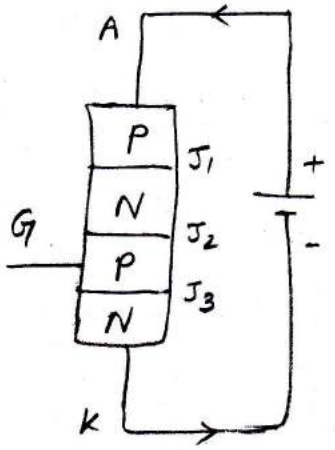
It is observed that reverse voltage increases but a very sm current flows.

At Reverse breakdown voltage (V_{BR}), the reverse current incr rapidly. (2m)

Forward blocking mode

Anode - +ve
Cathode - -ve
Gate - open.

J_1 & J_3 - Forward biased
J_2 - reverse biased.



A very small current flows from anode to cathode (will be mA)

This current is called foward leakage current.

In this mode, the thyristor is foward biased but it doesn turn-on.

When V_{AK} reaches V_{BO}, the SCR turns on. (2m)

Forward conduction mode.

SCR can be brought into conduction by the following

(i) When $V_{AK} > V_{BO}$

(ii) When gate drive is applied

(iii) When $\frac{dV}{dt}$ exceeds permissible value

(iv) When gate cathode junction is exposed to light.

(2m)

Latching current.

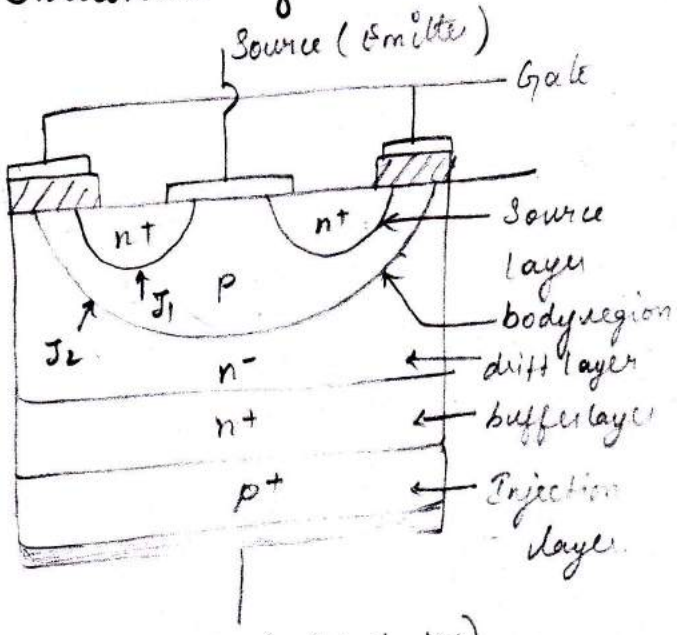
I_L is the minimum anode current required to bring the SCR into conduction (ie, on state) at the time of triggering. $I_L > I_H$.

Holding current

I_H is defined as the minimum anode current that is required by the SCR to keep it / maintain it in on state.

a) Explain the structure of IGBT with neat sketch.

i) **Structure of IGBT**



(or)

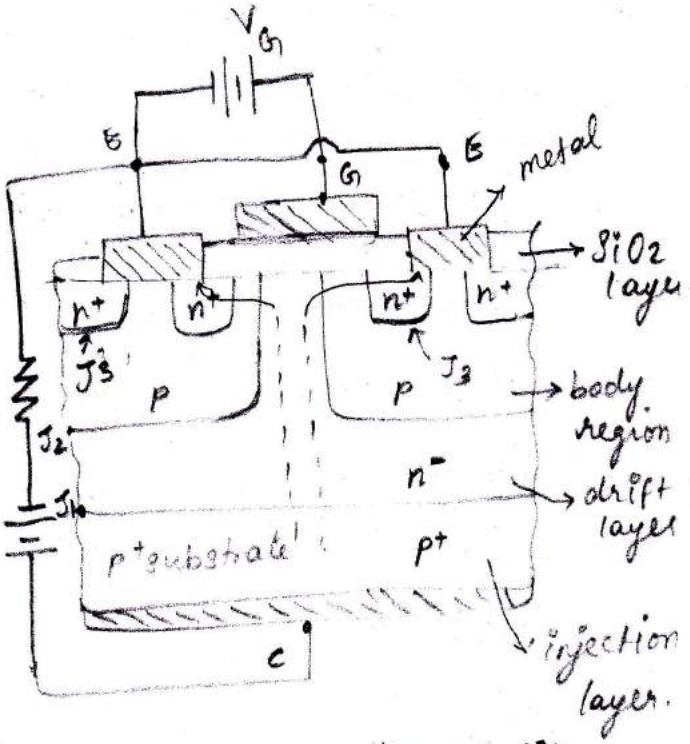


diagram (3)

The above figure shows the vertical crossection of n-channel IGBT.

IGBT is a combination of both BJT & MOSFET.

IGBT possesses high i/p impedance like a power MOSFET & has low on-state power loss as in a BJT.

The construction of MOSFET is similar in structure as power MOSFET except a thing.

The main difference in the structure is that the existance of p^+ layer that forms the drain of IGBT.

The n^+ buffer layer blw the p^+ drain contact & the n^- drift layer is not essential for the operation of IGBT.

IGBT's with buffer layer are termed as punch-through IGBT's whereas the IGBTs without buffer layer are termed as non-punch through IGBT

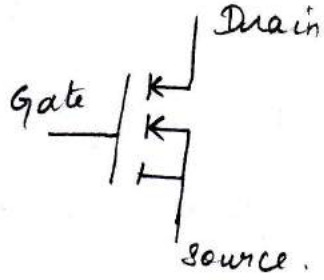
The n^- layer is called drift region

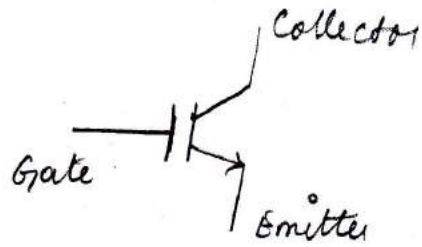
The thickness of n^+ layer determines the voltage blocking capability of IGBT

The p layer is called body of IGBT

The n^- layer in between p^+ & p regions serves to accomodate the depletion layer of pn^- junction ie, (J_2)

Symbols of an IGBT





Has 3 terminals namely
gate
Collector (drain)
emitter (source)

The symbol of an IGBT is like to n-channel p Mosfet, but with an addition of an arrowhead in the drain.

explanation - (4m)

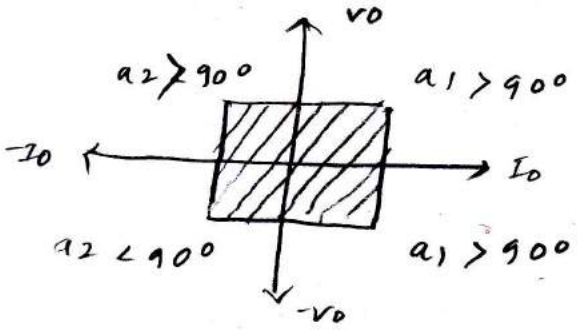
With neat diagram explain the operation of dual converters with necessary waveforms.

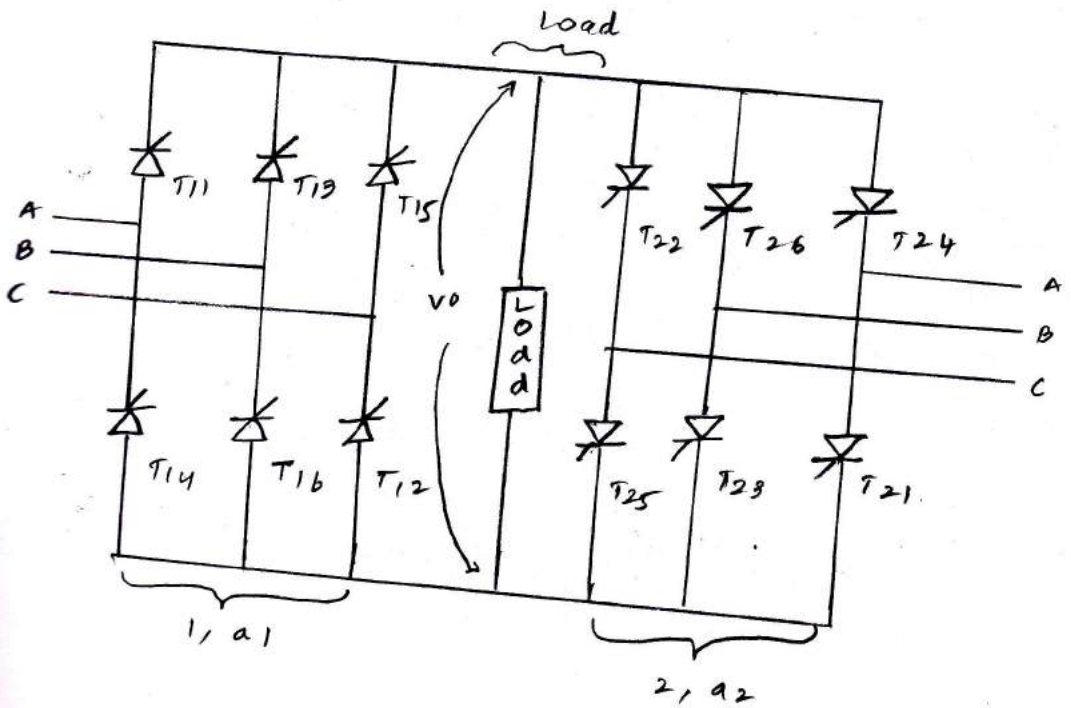
Dual converters

semiconverter are single quadrant converters thus a fully converters operates as a rectifier in first quadrant (both V_o, I_o positive) from $\alpha = 0°$ to $90°$ and as an inverter (V_o negative but I_o positive) from $\alpha = 90°$ to $180°$ in fourth quadrant this shows that a fully converter can operate as a two quadrant converter.

An arrangement using two full converters in antiparallel are connected to the same dc load is called dual converters.

There are two functional modes of dual converter, one is non circulating-current mode and other is circulating current mode.





only one converter is in operation at a time

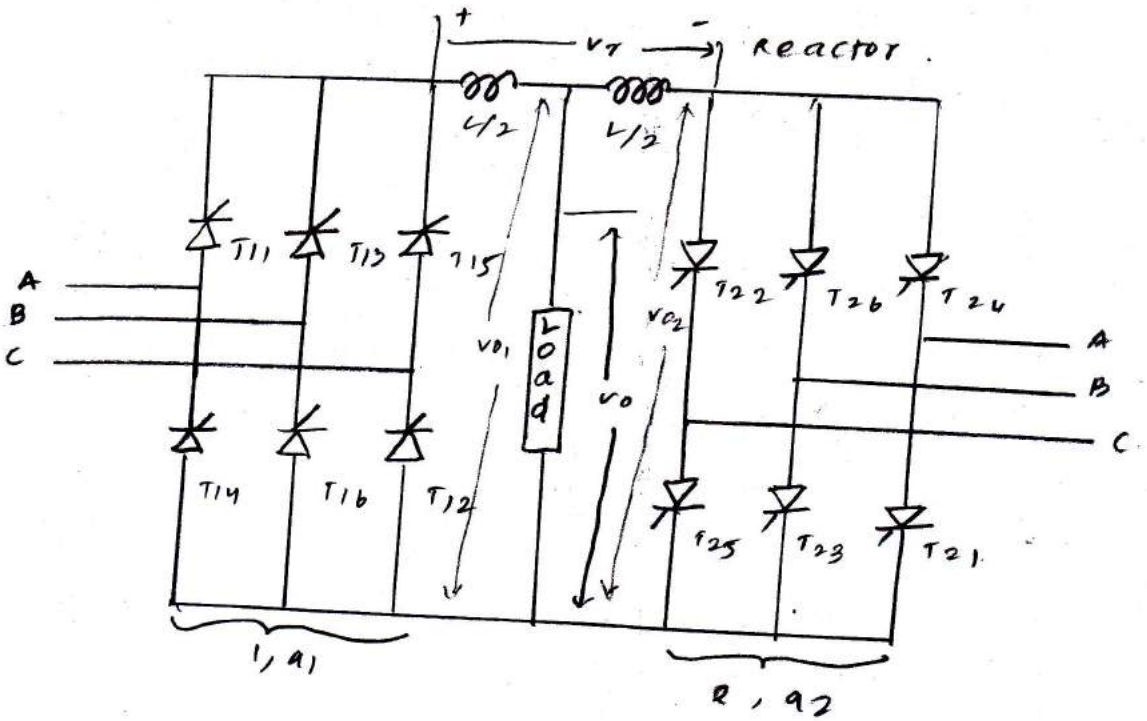
Dual converter without circulating current : with non circulating current dual converter, only one converter is in operation at a time and it alone carries the entire load current. only this converter receives the firing pulses from the triggering control.

only one converter is in operation at a time whereas the other converter is idle.

with non circulating current mode of dual converter the load current may be continous or discontinous. The control circuitry for the dual converter is so designed as to give satisfactory operation during continous as well as discontinous load current.

Dual converter with circulating current :

In the circulating current mode of dual converter, a reactor is inserted in between converters 1 and 2. this reactor limits the magnitude of circulating current to reasonable value.



The firing pulse of two converters are so adjusted that $\alpha_1 + \alpha_2 = 180^\circ$. As per example, if firing angle of converter 1 is 60° then firing angle of converter 2 must be 120°. Therefore, for these firing angles, converter 1 is working as a rectifier and converter 2 as an inverter. Though the output voltage at the terminals of both converter 1 and 2 has the same average value and also has the same polarity, their instantaneous output voltage waveforms, however, are not similar as shown by v_{01} and v_{02}. (b) As a consequence of it limited by the reactor. If the load current is to be reversed, the role of two converters is interchanged. This means that the converter 1 is now made to act as inverter by making its firing angle greater than 90° and converter 2 is made to work as rectifier by making its firing angle as less than 90° such that $\alpha_1 + \alpha_2 = 180^\circ$. The normal delay period of 10 to 20 msec, as required in circulating current free operation. faster.

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